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- **IEEE ELECTRON DEVICE LETTERS, vol. 13, no. 1, January 1992 NEW YORK, USA, pages 53-55, XP 000240817 KUEING-LONG CHEN ET AL. 'A SUBLITHOGRAPHIC ANTIFUSE STRUCTURE FOR FIELD-PROGRAMMABLE GATE ARRAY APPLICATIONS'**

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Description

[0001] The present invention relates to solid-state storage devices, particularly one-time programmable read only memory (OT-PROM) cells, arrays and circuits including the same, and methods for programming and reading such arrays.

[0002] In recent years, along with the development of information/video industries, media and devices for storing information have been extensively developed. Of these media and devices, storage devices such as DRAMs, SRAMs, and the like have large storage capacities even though they have compact, lightweight, and low-power structure, and allow high-accuracy read/write operations at high speed. For these reasons, these devices are used in equipment in various fields.

[0003] Also, recently, a storage device, so-called a flash memory, which is programmable and can hold information, has received a lot of attention. This storage device is superior to the DRAM in terms of the degree of integration.

[0004] On the other hand, an OT-PROM (one time PROMs) in which information can be written only once has been proposed in Japanese Laid-Open Patent Application No. 62-188260 (inventor: Levi Gersburg (phonetic)) and Japanese Laid-Open Patent Application No. 62-49651 (inventors: Brian E. Cook, Douglas P. Berlet (phonetic)). In the arrangement of the OT-PROM, a wiring metal is connected in series with a main electrode (the source or drain for a MOSFET; the emitter for a bipolar transistor) of a transistor via an a-Si layer. By changing the a-Si layer from a high-resistance state to a low-resistance state, a storage operation is achieved.

[0005] However, a storage device such as a DRAM using a semiconductor has the following problems.

1. Semiconductor storage devices represented by DRAMs and SRAMs suffer a high rate of chip cost increase along with an increase in storage capacity, and also suffer higher bit cost than those of floppy disks, magnetic tapes, and CD-ROMs. For these reasons, such a storage device cannot be actually used as a high store capacity storage medium.
2. At present, the storage capacity is at the 256-Mbit level even at the research level, and is insufficient as an information volume for images.
3. When information is stored in a DRAM or SRAM, the DRAM or SRAM must be kept supplied with a power supply voltage, and it is difficult to apply it to portable equipment. Under these circumstances, a battery built-in device is applied to such equipment.

[0006] On the other hand, a flash memory which is superior to a DRAM in terms of degree of integration, also has the following problems.

1. Since a charge is written in or erased from a floating gate by injection of a Ford-Nordheiom (FN) tunnel current, hot electrons, or the like, the reliability of an insulating layer which is subjected to a charge input/output operation is degraded as the number of times of use increases.
2. The FN tunnel current density, J, is expressed by:

$$J = \alpha E^2 \exp(-\beta/E) \quad (1)$$

where E is the electric field to be applied to the insulating layer, and α and β are constants. From equation (1), a large current flows when the electric field strength is large. However, as the floating gate potential changes, the current decreases exponentially. Therefore, the write or erase time per bit is as long as about 100 μs to 10 ms, resulting in poor operability of the storage device.
3. The FN tunnel current strongly depends on the film quality and thickness of the insulating film, and the proper write or erase time undesirably varies among samples and bits. For this reason, in practice, after chips are manufactured, the chips are classified into a plurality of groups in an inspection process, and are operated at timings suitable for these groups. Thus, the load on the inspection process is heavy, resulting in high cost.
4. As the storage capacity increases, the floating gate area decreases. For this reason, the floating gate capacity decreases proportionally, and the floating gate potential changes largely even by a small leakage current. Therefore, in order to assure a desired capacity, an affordable reduction in floating gate area is limited, and this limitation disturbs an increase in capacity.

[0007] Furthermore, the OT-PROM in which information can be written only once is excellent in that the state after information is written is permanent . However, one kind of OT-PROM has required an a-Si layer and a contact area between the a-Si layer and a wiring layer per bit. In a semiconductor process, formation of contact holes is difficult to achieve as compared to formation of line patterns. Even if a 0.8-μm rule process is used, the contact size is on the 1-μm^2 order which is about 20% larger than 0.8 μm. Since the wiring width must be larger than each contact hole, the area per bit cannot be reduced. For these reasons, it is difficult to realize a large storage capacity in the proposed memories. Also, since a large current flows through the a-Si layer in a write operation, the consumption power is high, and it is difficult to apply such a memory to portable equipment.

[0008] Another kind of OT-PROM is described in European Patent Application EP-A-0089457 in which there is disclosed a single gate PMOS transistor cell wherein the gate insulator has thinner and thicker portions adjacent the drain and the source, respectively. The gate electrode, channel and the thinner portion of the gate

insulator adjacent to the drain serve as an antifuse which is irreversibly changeable from a high resistance state to a low resistance state.

[0009] Yet another kind of OT-PROM is described in published Japanese Patent Application JP-A-51-147135. The principal features of the memory cell, a double insulated gate FET, are recited in the preamble of claim 1 attached. However, in the case of this published disclosure, the antifuse provided is constituted by the floating gate, the channel and a thinner portion of the floating gate insulator layer at the source end of the channel.

[0010] The memory cell of the present invention is characterised in that:

the capacitance between the floating gate and the channel is greater than the capacitance between the control gate and the floating gate and the antifuse is formed of the control gate, the control gate insulator layer, and the floating gate.

[0011] Other aspects of the present invention include the memory arrays, circuits, and methods of programming and of reading such arrays as set forth in the appended claims.

[0012] Insofar as in the arrays claimed an antifuse is provided in each cell at the intersection of each wordline and bit line, it is mentioned that there is disclosed a matrix wired array of antifuses in IEEE Electron Device Letters, Vol. 13, No. 1, January 1992 pages 53-55, the article "A Sublithographic Antifuse Structure for Field Programmable Gate Array Applications" by Chen, K.L. et al. A detailed description of antifuse construction is given therein.

[0013] Insofar as the memory cell claimed is a transistor having a source, a drain, a channel, an insulated floating gate and an insulated control gate it is acknowledged that United States Patent US-A-4,332,077 discloses an EEPROM having the same. In the transistor cell described therein the control gate overlaps with both a portion of the floating gate and a portion of the channel at the drain end thereof. The capacitance between the floating gate and the channel is greater than that between the control gate and the floating gate. The memory cell is programmed by causing a transfer of charge between the floating gate and the channel by Ford-Norheim tunnelling. The control gate insulator remains insulative, having at all times a high resistance state. The same is true of the floating gate insulator.

[0014] Since an ON current of a transistor does not flow via an anti-fuse unlike in a conventional anti-fuse ROM, an operation error caused by heat can be prevented, and high reliability can be guaranteed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015]

Fig. 1 is a circuit diagram showing the circuit arrangement of a storage device according to the present invention;

Fig. 2 is a timing chart showing the write operation according to the first embodiment of the present invention;

Fig. 3 is a timing chart showing the read operation according to the first embodiment of the present invention;

Fig. 4 is a plan view showing a cell portion according to the first embodiment of the present invention;

Figs. 5A and 5B are sectional views showing the cell portion according to the first embodiment of the present invention;

Figs. 6A to 6D are sectional views showing the processes in the manufacturing method according to the first embodiment of the present invention;

Figs. 7A and 7B are sectional views showing a cell portion according to the second embodiment of the present invention;

Figs. 8A to 8C are sectional views showing the processes in the manufacturing method according to the second embodiment of the present invention;

Figs. 9A to 9C are respectively a plan view and sectional views showing a cell portion according to the third embodiment of the present invention;

Fig. 10 is a perspective view showing a process in the manufacturing method according to the third embodiment of the present invention;

Fig. 11 is a perspective view showing a process in the manufacturing method according to the third embodiment of the present invention;

Fig. 12 is a perspective view showing a process in the manufacturing method according to the third embodiment of the present invention;

Fig. 13 is a perspective view showing a process in the manufacturing method according to the third embodiment of the present invention;

Fig. 14 is a perspective view showing a process in the manufacturing method according to the third embodiment of the present invention;

Fig. 15 is a perspective view showing a process in the manufacturing method according to the third embodiment of the present invention;

Fig. 16 is a perspective view showing a process in the manufacturing method according to the third embodiment of the present invention;

Fig. 17 is a circuit diagram showing an equivalent circuit of a cell portion according to the fourth embodiment of the present invention;

Fig. 18 is a plan view showing the cell portion according to the fourth embodiment of the present invention;

Fig. 19 is a sectional view showing the cell portion according to the fourth embodiment of the present invention;

Fig. 20 is a sectional view showing the cell portion according to the fourth embodiment of the present invention;

Fig. 21 is a sectional view showing the cell portion

according to the fourth embodiment of the present invention;

Fig. 22 is a circuit diagram showing an equivalent circuit according to the fifth embodiment of the present invention;

Fig. 23 is a block diagram of a system upon application to a PC card according to the sixth embodiment of the present invention; and

Fig. 24 is a perspective view showing a storage device according to the seventh embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] According to one preferred aspect of the present invention, source and drain semiconductor regions of a second conductivity type are formed each end of a channel semiconductor region of a first conductivity type, and a gate electrode structure is formed over the channel region. Furthermore, the gate electrode is designed to have a structure having two stacked gate electrodes, namely a floating gate and a control gate. In addition, by utilising the difference between the resistances between the stacked gate electrodes, information is stored.

[0017] When the transistors are arranged in a matrix as needed, a large-capacity memory can be realized.

[0018] As will be described later, by improving the structure of the transistor, the structure of the stacked gate electrode, and the like, the device performance can be further improved.

[0019] The preferred embodiments of the present invention will be described in detail hereinafter with reference to the accompanying drawings.

(First Embodiment)

[0020] Fig. 1 shows an equivalent circuit of fundamental blocks of a storage device according to the present invention. The circuit shown in Fig. 1 has memory cells 11, 12, 13, 14, 21, 22, 23, 24, 31, 32, 33, 34, 41, 42, 43, and 44, and this embodiment exemplifies a 4 × 4 cell structure for the sake of simplicity (note that the detailed structure of each cell will be described in detail later).

[0021] Each memory cell has a control gate 1 (serving as a floating gate 2, a channel 3, defined in a well or island, a source 5 and drain 6 forming thus a double insulated gate FET. The control gates of the memory cells of each row are connected via a word line 4. The sources and drains of the cells are connected in series with each other in units of columns. These cells are connected to a column decoder 7 as means for selecting each read column, a column decoder 8 as means for selecting each write bit line, a row driver 9 for driving each word line, a row decoder 10 for selecting each word line, a sense amplifier 15, and a buffer amplifier 16. Column address buffers 17 and 18 supply address inputs 20 to the column decoders 7 and 8. Switches SW1 to SW13 comprise MOSFETs. Of these switches, the switches SW9, SW10, SW12, and SW13 are ON/OFF-controlled by pulses $\phi1$, $\phi2$, $\phi3$, $\phi4$, and $\phi5$. The circuit receives a row address strobe signal ($\overline{RAS}$) 26, a column address strobe signal ($\overline{CAS}$) 27, a write enable signal ($\overline{WE}$) 28, and an input data signal (D_{IN}) 29, and outputs an output data signal (D_{OUT}) 30. Note that $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ are shown in Fig. 1.

[0022] The operation of this storage device will be described below. In this device, two different address signals are time-divisionally input from a single input pin. After the column address is determined, the $\overline{CAS}$ signal 27 changes from high level to low level to fetch the column address into the chip. After the row address is determined, the $\overline{RAS}$ signal 26 changes from high level to low level to fetch the row address into the chip. With this control, the number of address pins can be halved. Whether the chip is in a read or write mode is determined depending on high or low level of the $\overline{WE}$ signal 28.

[0023] In the read mode, after an elapse of a predetermined period of time from the change in $\overline{RAS}$ signal, significant output data is obtained from a D_{OUT} terminal 30. In the write mode, data is written from a D_{IN} terminal 29.

[0024] The write operation will be described in detail below with reference to the timing chart shown in Fig. 2. The power supply voltage of this chip is set to be 3.3 V to achieve low power consumption. In Fig. 2, CG1, CG2, CG3, and CG4 represent the first, second, third, and fourth word line potentials in Fig. 1. Also, BL1, BL2, BL3, and BL4 represent the pulses respectively input to the switches SW5 to SW8 as n-MOSFETs. Fig. 2 exemplifies pulses generated when information is written in the cell 21 in the storage device of this embodiment. Before the write operation, the column decoder-1 8 respectively sets the pulses BL1, BL2, BL3, and BL4 at high level, low level, low level, and low level, thereby setting the switch SW5 in an ON state, and setting other switches SW6, SW7, and SW8 in an OFF state. In this state, the well potential of the first column having a write target cell is held at the GND level as the low-potential reference voltage, and the well potentials of the remaining second to fourth columns are set in a floating state.

[0025] On the other hand, the switches SW9, SW10, SW11, SW12, and SW13 also comprise n-type MOSFETs, and pulses $\phi1$, $\phi2$, $\phi3$, $\phi4$, and $\phi5$ are respectively set at low level, high level, high level, high level, and low level, as shown in Fig. 2. The switches SW1 to SW4 comprise p-type MOSFETs, and all pulses from the column decoder-2 7 are set at low level, thereby holding the source and drain potentials of the respective cells at the GND potential as the low-potential reference voltage.

[0026] Then, the row driver 9 applies a pulse with an amplitude of 10 V to only a word line connected to the write target cell 21. In this case, although the power supply voltage is 3.3 V, since no current flows, a high voltage

can be easily generated by a booster circuit in the chip. Upon application of this write pulse, a bias of about 6.6 V is applied across the control gate 1 and the floating gate 2 of the cell 21, and the resistance between the control gate 1 and the floating gate 2 changes from a high-resistance state to a low-resistance state in several ten ns, thus completing the write operation. Even when the above-mentioned pulse is applied across the control gate and the floating gate of each of the cells 22, 23, and 24 connected to the same word line, since only a bias as low as about 0.1 to 0.5 V is applied across these gates, the resistance between the control gate and the floating gate of each cell remains in a high-resistance state. For this reason, no information is written in these cells. This is because the voltage is mainly applied to the well and the substrate and is not applied across the control gate and the floating gate since the switches SW6 to SW8 are set in an OFF state, and the well potentials of the second, third, and fourth columns are set in a floating state, as described above. After the completion of the write operation, the word line potential is reset to 0 V, as indicated by CG2 in Fig. 2.

[0027] As has been described above, the storage device of the present invention is a novel one since the gate structure of the transistor provided to each cell has a stacked structure of a floating gate and a control gate, and the storage device achieves the write operation by changing the resistance between the floating gate and the control gate (to a low resistance) by a pulse applied to the control gate.

[0028] The read operation of the present invention will be described below with reference to the timing chart shown in Fig. 3. The transistors constituting the respective cells are assumed to be p-type MOSFETs, and their threshold value is set to be -1.8 V. In this embodiment, each cell portion is assumed to be a p-type MOSFET but may be an n-type MOSFET.

[0029] Assume that a column to be subjected to the read operation is the first column in Fig. 1, information has already been written in only the cell 21 in this column, and no information is written in other cells 11, 31, and 41.

[0030] In order to read out information from the first column, the column decoder-2 7 applies pulses for setting the transistor of only the switch SW1 in an ON state, and setting the transistors of other switches SW2, SW3, and SW4 in an OFF state to the gates of the switches. In the read operation, the switches SW12, SW13, and SW5 are set in OFF, ON, and ON states, so that the well potential of the column to be subjected to the read operation is fixed at the highest potential when the cell transistor is a PMOS. Needless to say, when the cell transistor is an NMOS, the fixed well potential is the lowest potential.

[0031] First, the pulse $\phi 1$ is set at high level to precharge the source-drain paths of the cells 11, 21, 31, and 41 to V_{CC} level. This operation can be achieved when all the word lines are set at 0 V and the p-type MOSFETs of the respective cells are set in an ON state. The pulse $\phi 1$ is set at low level, and a pulse CG1 of an amplitude of 3.3 V is applied to a word line connected to the cell 11, as shown in Fig. 3, so as to read out information from the cell 11. Since no information is written in the cell 11, the floating potential is 1.1 V which is determined by dividing the capacitances of the control gate and the floating gate of the cell. As described above, the threshold value of the p-type MOSFET of this embodiment is set to be -1.8 V, and even when the above-mentioned pulse is applied, the p-type MOSFET of the cell 11 remains in an ON state. Therefore, when the pulse $\phi 3$ is applied, since all the p-type MOSFETs of the first column are in an ON state, the output from the sense amplifier 15 decreases, as indicated by 35 in Fig. 3, and it is determined that no information is written in the cell 11. Next, the pulse $\phi 1$ is applied again to pre-charge the cells, and thereafter, the pulse CG2 is set at high level to read out information from the cell 21. Since the pulse has an amplitude of 3.3 V, and information has already been written in the cell 21, the control gate and the floating gate of the cell 21 are connected to each other in a low-resistance state, and the pulse of 3.3 V is directly applied to the cell 21. Therefore, the p-MOSFET of the cell 21 is set in an OFF state. As a result, even when the pulse $\phi 3$ is applied, the sense amplifier output is kept at high level, as indicated by 36 in Fig. 3, and it is determined that information is written in the cell 21. By repeating the same operation, the outputs from the cells 31 and 41 are at low level, as indicated by 37 and 38 in Fig. 3, and no information is written in these cells.

[0032] After the read operation, the pulses $\phi 2$, $\phi 3$, and $\phi 4$ are set at high level, and the pulses $\phi 1$ and $\phi 5$ are set at low level, thereby setting not only the control gates of the cells but also the sources, drains, and the wells of them at 0 V. With this operation, the floating gate potential is stably reset to 0 V as an initial state, thus preventing an operation error. More specifically, in a standby state, all the sources, drains, control gates, and wells are set at 0 V, and even when a small leakage current flows through the floating gate, the gate is always automatically reset to 0 V, thus stabilizing the operation.

[0033] Note that a more stable write operation is assured if the following relations are satisfied:

$$\frac{C_{FG}}{C_{FG} + C_{CG}} V_1 \geq V_{BD}$$

$$\frac{C_{CG}}{C_{FG} + C_{CG}} V_2 < V_{th}$$

$$V_2 > V_{th}$$

where V_{BD} is the voltage across the floating gate 2 and the control gate 1 when the resistance between them

changes from a high-resistance state to a low-resistance state, V_{th} is the threshold value of the MOSFET,

C_{FG} is the capacitance formed between the floating gate 2, and the source/drain region and the well region of the MOSFET, C_{CG} is the capacitance formed between the floating gate 2 and the control gate 1, and V_1 and V_2 are the voltages to be applied to the control gate respectively in the write and read modes.

[0034] Fig. 4 is a plan view of the memory cell portion of the present invention. The cell portion comprises word lines 51, 52, and 53 consisting of poly-Si and W-polyside, p^+-type layers 54 and 55 which form the sources and drains of the p-type MOSFETs, floating gates 56 and 57 consisting of poly-Si, and channel portions 58 of the p-type MOSFETs. Figs. 5A and 5B respectively show an X_1-X_1' section and a Y_1-Y_1' section of Fig. 4. The same reference numerals in Figs. 5A and 5B denote the same parts as in Fig. 4, and a detailed description thereof will be omitted.

[0035] A gate insulating layer 59 for the p-type MOSFETs preferably consists of: a combination of a nitride film, and a thermal oxide film of Si or an oxide film formed by Lp-CVD to achieve a large capacity; a thermal oxynitride film formed in an atmosphere of O_2, NH_3, and N_2O; or Ta_2O_5 with a high dielectric constant. In this embodiment, a 10 nm (100-Å) thick film with an effective dielectric constant of 5 was formed by combining an oxide film and a nitride film, and was used as the insulating film.

[0036] The cell portion also comprises a p-type substrate 60, and a high-concentration n^+-type layer 63 formed below the n-type well. When the number of p-type MOSFETs to be connected in series with each other is small, if the resistance of the n-type channel sufficient, the n^+-type layer 63 is not always required. An insulating layer 61 is formed between the floating gate and the control gate. In this embodiment, a 5nm (50-Å) thick poly-Si film is formed to serve as the insulating film 61 by thermal oxidation of the floating gate. With this structure, the capacitance per unit area between the control gate and the floating gate is higher (about 1.5 times) than that between the floating gate and the lower Si layer. However, as can be seen from Figs. 4 to 5B, the floating gate is formed to have an area larger than the overlapping area of the control gate and the floating gate, and the practical capacitance between the floating gate and the underlying Si layer is set to be higher than that between the control gate and the floating gate. Thus, a desired voltage is applied across the control gate and the floating gate upon application of a write pulse.

[0037] The method of manufacturing the structure according to the present invention will be described below with reference to Figs. 6A to 6D. Note that the same reference numerals in Figs. 6A to 6D denote the same parts as in Figs. 4 to 5B.

[0038] As the p-type Si substrate 60, a substrate having an impurity concentration of 10^{14} to 10^{17} cm^{-3} can be used. In this case, in consideration of the width between wells to be divided, and the capacitance formed in each well, a substrate having an impurity concentration of 10^{16} cm^{-3} is preferable. As shown in Fig. 6A, a field oxide film 64 for element isolation is formed by a selective oxidation or modified selective oxidation method (when an Si film is oxidized after a groove is formed in the Si film where a field oxide film is to be formed by etching, the bird's beak is narrowed, and the isolation width can be decreased). Thereafter, patterning for forming the n-type well 58 is performed, and a well having an impurity concentration about 2 to 7 times the substrate concentration is formed by ion implantation. In this case, in order to assure the withstand voltage between adjacent n-type wells, the depth of the well is level with the bottom level of the field oxide film 64, i.e., the well is considerably shallower than a conventional one. In the next step, as shown in Fig. 6B, an 8.5 nm (85-Å) thick thermal oxide film is formed by Wet oxidation at 750°C to 1,100°C, and is subjected to a heat treatment in an NH_3 atmosphere at 950°C to 1,100°C for 90 seconds, and in an O_2 or N_2O atmosphere at 1,150°C for 90 seconds, thus essentially forming an SiON film having a thickness of about 10 nm (100Å). Then, 400 nm (4,000-Å) thick poly-Si films 57 and 66 as the first layer are formed by Lp-CVD, and are subjected to ion implantation and annealing to dope an impurity in the poly-Si films. Thereafter, n^+-type layers 65 serving as the source and drain of the n-type MOSFET, and p^+-type layers 54 serving as the source and drain of the p-type MOSFET are formed. In order to relax electric fields at the source and drain terminals upon miniaturization, the n- and p-MOSFETs preferably have LDD and GOLD structures formed in low-temperature operations, respectively.

[0039] Subsequently, as shown in Fig. 6B, the oxide film formed on the poly-Si surface is peeled using dilute hydrogen fluoride. After the peeling, a chemical oxide film having a thickness of about 1 nm (10Å) to 5 nm (50 Å) is formed in pure water added with ozone (O_3), an acid (H_2SO_4, HCl) added with hydrogen peroxide water, or alkali (NH_4OH), and is subjected to a heat treatment in a high-purity Ar or N_2 atmosphere at 500°C to 600°C for 30 minutes. When the thickness of the oxide film is to be slightly increased, an O_2 atmosphere is also mixed. With this operation, a very thin oxide film is formed although it has a thickness different from that formed by an impurity in the poly-Si surface of the first layer. On this wafer, a poly-Si film as the second layer is formed by Lp-CVD again. An impurity is then doped in the same manner as in the previous process, and the resultant structure is patterned to form the word lines 51. When the word line length is large, W-polyside or the like is preferably used to achieve a low resistance. Finally, as shown in Figs. 6C and 6D, an insulating interlayer 70 such as BPSG, a contact 67, a metal wiring line 68, a passivation film are formed as in a conventional LSI process, and the resultant structure is pat-

terned to form a pad portion 69, thus completing the manufacturing process of this embodiment. The number of masks used for forming the structure of this embodiment is half or less that required for manufacturing conventional memories such as DRAMs, SRAMs, flash E^2PROMs, and the like. Therefore, not only the area per bit is decreased, but also the processes are very simple, resulting in high yield and low cost. In the description of the manufacturing method of this structure, a single well structure has been exemplified. However, the present invention is not limited to this. The method of the present invention is also effective for a double well structure including n- and p-type wells, a structure formed with a channel stop layer in an isolation portion, and a structure adopting trench isolation in some cases.

[0040] In this structure, as the insulating layer between the first and second poly-Si layers, the chemical oxide film is annealed at a low temperature (500°C to 600°C) to form a film which has a withstand voltage about half or less than that of a thermal oxide film of bulk Si, and suffers only small variation. In this case, when an oxygen ion-implantation film is formed on the surface of the first poly-Si layer, an oxide film having a defective layer containing oxygen is obtained, and the withstand voltage is lowered with high controllability. In this case, in place of a chemical oxide film, a thermal oxide film having a thickness of about 10 nm (100Å) may be formed to assure a desired withstand voltage, and the capacitance can be lowered as the film thickness can be increased.

[0041] As described above, a memory according to the first embodiment of the present invention has the following merits:

1) The memory structure is simple, and the area of one cell portion is determined by only the word line and the patterning precision of an Si active layer. Therefore, since the area per cell can be equal to or smaller than that of a conventional memory without forming a contact, the bit cost can be lowered.
2) The number of masks required for forming this structure is about half that for DRAMs, SRAMs, flash RAMs, and the like, thus achieving further cost reduction. Also, since processes are simple, problems of dust, and pattern errors occur, thus improving the yield.
3) The write operation is achieved by breakdown of the insulating layer between the first and second poly-Si layers. Since the withstand voltage of the poly-Si oxide film is low due to the presence of the C-Si oxide film, and the withstand voltage can be stably set to be a desired value with high controllability upon combination with a new process technique such as a chemical oxidation method, or an oxygen doping method, write errors hardly occur.
4) Written information is permanent. Therefore, neither a power supply to be connected to a memory nor a complicated operation such as a refresh operation are required.
5) The write time is very short, several 10 ns or less
6) Since the read and write states do not so strongly depend on environmental conditions (flash memories, DRAMs, and the like strongly depend on a leakage current), application variations can be extensively explored.

(Second Embodiment)

[0042] The second embodiment of the present invention will be described below with reference to Figs. 7A to 8C. An Si wafer was used as the substrate of the first embodiment, while in the second embodiment, an SOI substrate was used. Figs. 7A and 7B show the sectional structures (corresponding to Figs. 5A and 5B) of a memory cell portion, and Figs. 8A to 8C show the manufacturing method. Note that the same reference numerals in Figs. 7A to 8C denote the same parts as in Figs. 4 to 6D showing the first embodiment, and a detailed description thereof will be omitted. An SOI substrate 71 can use a high-quality SOI wafer such as SIMOX, a laminated SOI wafer, an SOI wafer which is manufactured by laminating, on a wafer having an insulating layer surface, a wafer which is formed by forming a porous layer on an Si surface, and forming an epitaxial film on the porous surface, and the like. The conductivity type of the substrate may be either n or p conductivity type, as long as the bias of the substrate is controlled so as not to turn on a parasitic MOS transistor formed via an SOI oxide film 72 (a MOS transistor formed when the oxide film 72 is considered as a gate insulating layer). Transistors in the cell portion are isolated in an island pattern, as indicated by 76 in Fig. 7A.

[0043] With this structure, an isolation width 73 in a direction parallel to the word lines can be smaller than that obtained using conventional selective oxidation or modified selective oxidation, and the area per bit can be further reduced. For this reason, the chip size can be reduced, thus attaining low cost and high yield.

[0044] Adjacent wells are completely isolated by an insulating layer, and the operation can be stabilized.

[0045] As can be seen from Figs. 7A and 7B, since a channel portion 76 and a floating gate portion 56 of a TFT in the cell portion are vertically stacked, a step between adjacent cells undesirably becomes large. For this reason, an insulating layer 74 for planarization is formed between adjacent cells, so that word lines 75 can be formed flat.

[0046] In the structure of the second embodiment, since the insulating layer is formed below the well, the capacitance of the well can be smaller than that obtained when a bulk substrate is used. As a result, in the write mode, the voltage between the control gate and the floating gate can be reduced for a non-write bit, write errors hardly occur, and the margin of the structure process can be widened.

[0047] The manufacturing method according to the

second embodiment of the present invention will be described below with reference to Figs. 8A to 8C. After n-type wells 77 and p-type wells 78 are formed in corresponding regions on the SOI substrate 71, regions 79 and 80 where n- and p-type MOSFETs are to be manufactured are patterned. Then, the first poly-Si layer, and the sources and drains of the n- and p-type MOSFETs are formed following the same processes as in the first embodiment. After this, a TEOS insulating layer is formed, and is etched back to expose the upper portions of highest floating gates 57. After this, the oxide film on the surface of the first poly-Si layer is temporarily removed using dilute hydrogen fluoride, and a thin insulating layer is formed on the surface by chemical oxidation or low-temperature thermal oxidation, thus forming word lines 51. Thus, a planarized structure is obtained, and even when the pattern size of an upper metal wiring line 68 is reduced, high yield is attained.

(Third Embodiment)

[0048] The third embodiment of the present invention will be described below with reference to Figs. 9A to 9C.

[0049] Fig. 9A is a plan view of a memory cell, Fig. 9B shows an X_2X_2' section of this plan view, and Fig. 9C shows a Y_2Y_2' section of this plan view. The memory cell portion shown in Figs. 9A to 9C comprises word lines 91, 92, and 93, p^+-type diffusion layers 94 and 95 which serve as the sources and drains of p-type MOSFETs which are NAND-connected, floating gates 96 and 97 of the MOSFETs, n-type well layers 98 and 99 of the MOSFETs, a p-type substrate 81, n^+-type buried layers 82 and 83, a metal layer 101 (e.g., a Ta-based metal layer (Ta, TaN)) formed on the surface of each floating gate, and an insulating layer 102 including the metal. As can be seen from Figs. 9B and 9C, the floating gate 96 and 97 have opposing portions sandwiching the well layers 98 and 99 therebetween, respectively.

[0050] The outstanding feature of this structure as compared with the first and second embodiments is that the floating gates 96 and 97 are formed to have a small two-dimensional size so as to further reduce the cell area per bit in practice, and this structure is suitable for high integration. The reason why this structure is realized is that the transistors in the cell portion have three-dimensional structures, as shown in Fig. 9B, and the floating gate capacitance can be increased by utilizing not only upper portions 103 of the transistors but also side wall portions 104.

[0051] The second feature of the third embodiment will be described below.

[0052] This structure performs an SOI operation unlike a conventional bulk FET since the channel portions 98 and 99 are controlled by the parallel floating gates 96 and 97. Thus, since the effective carrier mobility is high, a high-speed read operation can be attained. In addition, a short channel effect which occurs upon miniaturization of the transistors can be suppressed, and a compact structure can be easily realized. This is because the channels are controlled by the two side gates, a high electric field is hardly applied, and the potential can be controlled. Therefore, the floating gate capacitance can be increased while simply reducing the two-dimensional size of the floating gate, thus realizing miniaturization. In addition, this transistor structure is most suitable for miniaturization.

[0053] As a problem of an SOI transistor, immediately after the transistor is switched from ON to OFF, the OFF operation is delayed by minority carriers remaining in the channel portion. However, in this structure, since the n^+-type layer is formed immediately below the channel, and can prevent the minority carriers from remaining, a higher-speed memory operation can be realized.

[0054] The third feature of the structure according to the third embodiment of the present invention is that the word lines 91 to 93 are patterned to have sizes larger than the floating gates 96 and 97. With this structure, upon patterning of the word lines, the surface of each floating gate can be prevented from being exposed to an etching plasma or the like, and the reliability of the insulating withstand voltage between the floating gates and the word lines can be further improved.

[0055] The fourth feature of the structure according to the third embodiment of the present invention is that the floating gates 96 and 97 are polyside films consisting of $TaSi_x$ to have a low resistance although each floating gate has a very small film thickness, and the high-quality insulating layer covering the metal is formed in self-alignment on the surface layer of each floating gate. In the memory structure of the present invention, the word line and the floating gate must be changed to a low-resistance state at a desired withstand voltage (e.g., 5 V), and a high-resistance state must be reliably maintained at 3 V. When the structure is adjusted to obtain a desired withstand voltage using a thin insulating layer, a leakage current begins to flow undesirably.

[0056] Therefore, it is important to form a dense film having a wide bandgap and high insulating characteristics in at least a portion of the structure. In this case, a metal layer of Ta, TaN, Ni, or Zr,

or a polyside layer is formed on the surface of the first poly-Si layer serving as the floating gate, and an insulating layer covering the metal layer is formed before formation of the second poly-Si layer. With this structure, an insulating layer which can assure a desired withstand voltage and can reduce the leakage current by 50% or more as compared to a conventional structure can be formed.

[0057] As a result, the error rate of the memory can be further lowered, and a memory with high reliability and high stability can be realized.

[0058] The method of manufacturing the memory according to the third embodiment of the present invention will be described below with reference to Figs. 10 to 16. Figs. 9A to 9C have exemplified a case wherein the memory structure is formed on a bulk Si substrate. How-

ever, since an equivalent structure can be formed even on an SOI substrate, and element isolation is facilitated, as has been described in the second embodiment, a description of the manufacturing method in Figs. 10 to 16 will be made using an SOI substrate. For the sake of descriptive simplicity, all cells are assumed to be p-type TFTs.

[0059] As shown in Fig. 10, an n^+-type layer serving as an n-type buried layer is formed on a region, where a p-type MOSFET is to be manufactured, on the surface of an SOI wafer 105. In this formation, an ion implantation method, as indicated by 106 in Fig. 10, a method in which an impurity is doped upon formation of a laminated wafer, or the like may be used. The film thickness of an Si layer which forms the n^+-type layer is preferably as small as possible, e.g. several hundred nm (several thousand Å).

[0060] As shown in Fig. 11, a 1-μm thick epitaxial film 108 is grown on an n^+-type layer 107. Film growth is preferably performed at low temperature and at high speed to prevent an impurity from being redistributed or auto-doped from the n^+-type layer. The epitaxial process may not often be required depending on the concentration of the epitaxial layer 108 since it increases cost.

[0061] As shown in Fig. 12, the layers 107 and 108 are patterned by anisotropic etching except for a portion 109 serving as an active layer. As the resist patterning, patterning on the order of 0.35 μm can be realized using a phase shift mask, modified illumination, or the like in an i-line stepper. Also, a stepper using an ArF excimer laser, EB lithography, and the like are suitable for micropatterning.

[0062] Subsequently, as shown in Fig. 13, an oxynitride film 110 is formed on the surface of the portion 109.

[0063] After the Si surface is oxidized in an O_2 atmosphere at 1,100°C for 50 seconds, it is then subjected to a treatment in an NH_3 atmosphere at 900°C for 60 seconds and in an N_2O atmosphere at 1,100°C for 30 seconds. After the insulating layer is formed, a poly-Si film serving as a floating gate and a metal layer are subsequently formed, as indicated by 111 in Fig. 13. More specifically, a 200 nm (2,000-Å) thick poly-Si film is formed at 620°C, and a 150 nm (1,500-Å) Ta film is grown thereon by sputtering. Then, phosphorus is ion-implanted in the surface of the Ta metal film, thus forming a Ta polyside layer containing metal Ta in its surface layer.

[0064] In the next step, as indicated by 112 in Fig. 14, a floating gate is patterned. Using the resist mask for the floating gate, boron is ion-implanted, as indicated by 113 in Fig. 14, thereby forming the source and drain.

[0065] Thereafter, as shown in Fig. 15, a TEOS layer 114 is formed, and after a resist is coated thereon, the layer is etched back to expose a surface 115 of the floating gate 112. After the exposed portion is washed to temporarily remove the insulating film on the surface layer containing Ta, the resultant structure is subjected to a heat treatment in an O_2 atmosphere at 200°C to 400°C, thereby forming an insulating oxide film containing a Ta metal. In the formation of the insulating oxide film, a method which also uses plasma irradiation may be used. The treatment is performed at a pressure of 4 Pa (30 mtorr) and at a temperature of 450°C while supplying Ar and O_2 gases at 300 and 8 sccm.

[0066] As shown in Fig. 16, the second poly-Si layer of a word line 116 is patterned to cover the insulating oxide film on the floating gate surface. Thereafter, an insulating interlayer such as BPSG is formed, and a contact hole, a wiring metal, and a passivation insulating layer are formed. Finally, a pad is etched to complete the sample chip.

[0067] In the above description, a structure in which a metal layer is stacked on the floating gate surface has been exemplified. Alternatively, an oxide film on a single poly-Si layer may be used as in the first and second embodiments.

[0068] When a layer having the same conductivity type as that of the well layer and a higher concentration than the well layer is formed on an upper edge portion of the well layer, changes in threshold value at the edge portion, and withstand voltage errors at the edge portion can be effectively prevented.

(Fourth Embodiment)

[0069] The fourth embodiment of the present invention will be described below with reference to Fig. 17 and Figs. 18 to 21. In the fourth embodiment, cells are arranged in a NOR matrix to improve characteristics associated with functions such as a random access function. Fig. 17 shows an equivalent circuit of several cells of a portion of the fourth embodiment. The circuit comprises buried bit lines 120 and 121, and buried source lines 122 and 123, which consist of diffusion layers. Contacts in units of cells are not formed to reduce each cell area. The bit and source lines are connected to a common source line 126 and main bit lines 127 and 128 via selection transistors 124 and 125 at a desired period according to an application, such as 8 bits, 32 bits, 64 bits, or the like. The circuit also comprises word lines 129, 130, and 131. A transistor 132 of the cell portion comprises an n-type MOSFET, and the diffusion layers of the source and drain have n^+ conductivity type. P-type well layers 133 and 134 are arranged in units of columns, and each two adjacent columns are isolated from each other.

[0070] The driving method for this device will be explained below. First, the write operation will be described. When a write bit is assumed to be the transistor cell 132 of Fig. 17, the buried source line 122, buried bit line 120, and p-type well 133 of this transistor are fixed at 0 V, and at least the well potentials (134 in Fig. 17) of other columns are set in a floating state. When a pulse of 10 V is applied to the word line 129, a voltage of about 6 V is applied across the floating gate of the transistor 132 and the word line 129, and the floating gate and the word line 129 change to a low-resistance state. On the

other hand, only a bias of 1 V or less is applied across the floating gate of a transistor 135 and the word line 129 since the well 134 is set in the floating state, thus maintaining a high-resistance state. The respective word lines are simultaneously driven to achieve parallel write operations.

[0071] The read operation will be described below. The threshold value of the n-type MOSFET is set at about 1.5 V. In the read operation, the well potentials of all the cells are fixed to be a lowest potential value, a voltage applied to a read word line is set at 2.0 V, and a voltage applied to non-read word lines is set at 0 V. Before reading, the respective bit lines are pre-charged to V_{DD} = 2 V to turn off the bit line switches (transistors) 125, and a word line to be selected is set at 2 V. The effective gate bias of a written cell becomes 2 V, the channel is turned on, and the bit line is set at the source potential, e.g., 0 V. On the other hand, the effective gate bias of each non-written cell becomes 1.2 V equal to or lower than the threshold value, since it is subjected to capacitance division with the floating gate. As a result, the transistor of the cell is set in an OFF state, and the bit line is kept at V_{DD}. A sense amplifier reads out changes in potential of these bit lines as in the first embodiment.

[0072] The two-dimensional structure and sectional structure of the fourth embodiment will be explained below with reference to Figs. 18 to 21. Fig. 18 is a plan view of a memory cell portion, Fig. 19 is a sectional view taken along a line X_3X_3' of Fig. 18, Fig. 20 is a sectional view taken along a line X_4X_4' of Fig. 18, and Fig. 21 is a sectional view taken along a line Y_3Y_3' of Fig. 18.

[0073] The same reference numerals in Figs. 18 to 21 denote the same regions as in Fig. 17, and a detailed description thereof will be omitted. This embodiment exemplifies a structure on a bulk Si substrate. However, as in the above-mentioned embodiments, the structure of this embodiment can also be manufactured on an SOI substrate. Wells in each two adjacent columns are isolated from each other by a selective oxide film 145, and floating gates in each two adjacent rows are isolated from each other by a thin selective oxide film 144. The buried bit lines are connected to metal wiring layers 146 and 147 for global bit lines at every 8 to 64 bits. Cells have floating gates 140 to 143.

[0074] When the NOR matrix of the fourth embodiment is adopted, various read and write methods are realized, and the memory of this embodiment can be applied to various systems.

(Fifth Embodiment)

[0075] The fifth embodiment of the present invention will be described below with reference to Fig. 22. The same reference numerals in Fig. 22 denote the same parts as in the above embodiments, and a detailed description thereof will be omitted. The circuit shown in Fig. 22 comprises a memory unit 150 described in the first embodiment, an SRAM unit 151, a scanning circuit 152 for sequentially reading out data from the SRAM, an EXOR circuit 153 for verifying the readout result of the memory of the present invention by comparing it with data from the SRAM, and a control circuit 154 for controlling the driving operation of the memory unit 150 in accordance with an output from the EXOR circuit. The SRAM unit 151 includes CMOS SRAM memory cell portions 155 which preferably comprise p-type MOS load memory cells since they require low consumption power. The SRAM unit 151 also includes MOS switches TR1, TR2, TR3, and TR4 for controlling the driving operations of the SRAM memory cells, common data lines 156, sense amplifiers 157, output buffers 158, and switches 159 for selecting the outputs from the output buffers. The EXOR circuit 153 comprises gates 160, 161, 166, 167, and 168, which are input to CMOS inverters via floating gates 162, p-type MOS transistors 163, and n-type MOS transistors 164. An output 165 from the first CMOS inverter is input to a gate 166 of the second CMOS inverter. An output 169 from the second CMOS inverter is input to the control circuit 154. Word lines 170, 171, and 172 are commonly arranged in the memory cell unit of the present invention, and the SRAM memory unit.

[0076] The operation method of the fifth embodiment of the present invention will be described below. Data are written in a desired column of the memory unit 150, and the same data are written in the SRAM cells in the SRAM memory unit 151. The memory unit 150 is set in a read mode, and the data in the column are sequentially read out using a sense amplifier 15. In synchronism with this read operation, the scanning circuit 152 reads out the corresponding bits from the SRAM cells of the SRAM memory unit 151 via the sense amplifiers 157, and these readout outputs are input to the gates 160 and 161 of the EXOR circuit 153. Since the output from the EXOR circuit 153 changes to high level when the values input to the gates 160 and 161 are different from each other, and changes to low level when they are equal to each other, whether or not data are normally written in and read out from the memory unit 150 can be checked based on the output from the EXOR circuit 153.

[0077] The EXOR circuit 153 is a CMOS circuit having multiple input gates via the floating gates, and can be manufactured based on a structure equivalent to that of the memory unit 150. In addition, the EXOR circuit 153 can realize high-performance processing using a smaller number of transistors. In this embodiment, an EXOR logic operation is executed. Alternatively, when input gates for 8-bit inputs are arranged via the floating gates to constitute the same CMOS inverters as above, a majority logic of input data can be realized by two transistors (n-type and p-type MOS transistors). By utilizing this majority logic, parity check operations of input and readout 8-bit data can also be attained.

[0078] The description of the operation of the circuit

shown in Fig. 22 will be continued. When an operation error is confirmed based on the output result 169, the SRAM data are written again in the next column of the memory unit 150. With this control, an operation for correcting write and read errors can be realized.

[0079] At least one bit of a data string may be assigned as an error check bit of the data string, and is confirmed when the data string is read out.

[0080] In the arrangement shown in Fig. 22, the SRAM memory unit has a memory size equal to that of one column of the memory unit 150. However, the present invention is not limited to this size. For example, the memory size may be increased to a level as a buffer memory to achieve high-speed random access and write operations. In the above description, the buffer memory comprises an SRAM. Alternatively, a DRAM, a flash memory, or the like may be arranged on a single chip to perform the above-mentioned operation.

[0081] The above-mentioned arrangement of the fifth embodiment has the following merits.

1) The error rate is very low.
2) Whether or not data is normally written can be confirmed on the chip.
3) The logic circuit for performing confirmation can be manufactured to have the same structure as that of the memory of the present invention without adding any new processes.
4) The logic circuit can be constituted by a smaller number of transistors than conventional logic circuits. For this reason, since a peripheral circuit can be realized in a small area, low cost and high performance can be attained.
5) Since a memory (SRAM, DRAM, flash memory, or the like) having a structure different from the memory structure of the present invention is incorporated, high-speed random access and write operations can be realized.

(Sixth Embodiment)

[0082] In the sixth embodiment of the present invention, the storage device of the present invention is applied to an external storage card (PC card) for, e.g., a personal computer.

[0083] An application of the present invention will be explained below. Fig. 23 is a diagram showing the relationship between a card and a system when the present invention is applied to a PC card.

[0084] In an existing notebook type personal computer or portable information communication equipment which can cope with a PC card, a device driver for a PC card to be used resides in a main memory. When a personal computer or portable information communication equipment uses a plurality of types of PC cards, the number of device drives to be resided in the main memory unit increases, and some application software programs cannot operate due to the large total capacity of the resident device drivers.

[0085] In a card constituted by using the memory chip of the present invention, a ROM unit is also arranged on the chip to store the device driver of the card and CIS information (card-information-structure), i.e., the type and capacity of the card, identification information and configuration information of the card, and the like. Thus, the card of this embodiment has a function of notifying card insertion, and executing down-loading in accordance with a device driver down-load instruction, as shown in Fig. 12.

[0086] An interface between the card and the main body has a 68-pin connector, and complies with a data bus width of 32 bits, a clock frequency of 16 MHz, a maximum data transfer rate of 60 Mbytes/s, and the like in accordance with the formats of PCMCIA (the standardization group in U.S.A.) and JEIDA (Japan Electronic Industry Development Association).

(Seventh Embodiment)

[0087] The seventh embodiment of the present invention will be described below with reference to Fig. 24. The seventh embodiment is directed to an IC card which inputs/outputs information based on light. The IC card comprises a storage device 180 of the present invention, a battery 181, a semiconductor laser 182, a photodetector 185, a control circuit 186 for controlling the storage device mounted on a board 179, the laser, and the photodetector, a transparent resin package 183, and a lens 184. The IC card of the present invention exchanges all kinds of information to be exchanged with an external circuit such as data to be written, data to be read out, control clocks, and the like on the basis of light, and all the remaining functions are executed by the control circuit 186 arranged on the board 179.

[0088] Although not shown in Fig. 24, alignment marks for aligning an optical system are formed on the board 179. When the IC card of this embodiment is set in a reader/writer of this card, the card is set at a desired position at high speed.

[0089] The IC card of this embodiment has the following merits.

1) Unlike a conventional IC card, the card of this embodiment has high reliability since it is free from a problem of a contact error of contact pins, a problem of low reliability of pins, and the like.
2) IC card mounting can be realized with very low cost since the IC card comprises a transparent resin package obtained by simple integral molding.
3) Since the modulation frequency of the semiconductor laser is high, information can be input/output at a high bit rate, and low consumption power can be attained.

(Eighth Embodiment)

[0090] The eighth embodiment of the present invention is directed to a storage device incorporating a programmable logic array in which the first poly-Si layer constituting the floating gates of the storage device of the present invention, and the second poly-Si layer constituting word lines are arranged in a matrix, a large number of AND gates and OR gates are arranged, and lines at each intersection of the matrix are changed from a high-resistance state to a low-resistance state to be substantially connected to each other, thereby freely setting a logic according to the intended application purpose of each user. The resistance between the lines can be changed to a low-resistance state in correspondence with the bias to be applied to lines arranged in a matrix.

[0091] When the storage device incorporates a programmable logic array, an operation according to the specifications of each user can be realized without changing the mask, thus reducing cost and shortening the delivery period to users.

[0092] The storage device of the present invention has the following effects: a larger capacity and a smaller cell area per bit than those of the conventional semiconductor storage device, permanently stable written information, low consumption voltage, low-voltage driving, storage and holding without any battery, high reliability, an easy driving method and high operability, high-speed read/write operations, a low error rate, wide use environments, a short manufacturing process, high yield, and high performance of a chip realized by integrating other types of storage devices, logic circuits, and the like as peripheral circuits on a single chip, and the like. The storage device of the present invention can be generally used not only as storage devices for computers but also as storage media for audio/video information, and can replace commercially available audio tapes, video tapes, CD-ROMs, and the like by utilizing higher performance characteristics than them. Also, the storage device of the present invention is suitable for an external storage device for portable equipment, electronic publishing, a controller, and an electronic video/image memory, e.g., a system which stores an output from a still video camera, FAX, copy machine, or the like in a card constituted by the storage device of the present invention to allow a user to easily carry video data.

[0093] As used herein, the abbreviation 'GOLD' means Gate-drain Overlapped Lightly Doped drain.

Claims

1. A one-time programmable read only memory (OTPROM) cell (11) comprising:

   a source (5;54;94);
   a drain (6;54;94);
   a channel (3;58;76;98) of opposite conductivity type to said source and drain;
   a floating gate (2; 56; 96) located over said channel;
   a floating gate insulator layer (59;104) disposed between said floating gate and said channel;
   a control gate (1;51;75-91) located over said floating gate; and
   a control gate insulator layer (61;101 & 102) disposed between said control gate and said floating gate;
   said cell having an antifuse (51,61,56; 75,61,56;91, 101,102,96) which is convertible irreversibly from a high-resistance state to a low-resistance state;

   characterised in that:

   the capacitance C_{FG} between said floating gate (2;56;96) and said channel (3;58;76;98) is greater than the capacitance C_{CG} between said control gate (1;51; 75;91) and said floating gate (2; 56;96) and said antifuse (51,61,56; 75,61,56; 91,101,102,96) is formed of said control gate (1;51; 75;91), said control gate insulator layer (61; 101 & 102), and said floating gate (2;56;96).

2. A cell according to claim 1 wherein the capacitance per unit area between said control gate (1;51;75;91) and said floating gate (2;56;96) is higher than that between said floating gate (2;56;96) and said channel (3;58;76;98), the area of said floating gate (2; 56;96) thus being larger than the overlapping area of said control gate (1;51;75;91) and said floating gate(2;56;96).

3. A cell according to claim 2 wherein said floating gate is interposed between said control gate and said channel leaving no area of direct overlap between said control gate and said channel.

4. A cell according to any of claims 1 to 3 wherein said source and drain are defined in a well (58;133) region of a semiconductor substrate (60;-), said channel being a part of said well, extending between said source and said drain.

5. A cell according to any of claims 1 to 3 wherein said source (54) and drain (54) are defined in an isolated portion (80) of a semiconductive active layer (77,78) on an insulative substrate (71), said channel being a part of said isolated portion (80) of said semiconductive active layer, extending between said source and said drain.

6. A cell according to either of claims 4 or 5 wherein said floating gate insulator layer (104;113) and said floating gate (96;112) extend vertically down each side of said channel (98;108) to increase the capac-

itance therebetween.

7. A cell according to any preceding claim wherein said floating gate insulator layer is of silicon oxynitride (SiON) and said floating gate is of doped polycrystalline silicon (poly-Si).

8. A cell according to any preceding claim, being once programmed and having thus said antifuse in said low-resistance state.

9. An OT-PROM memory array comprising:

a plurality of memory cells (11-44) arranged in rows and columns, each cell being a cell as claimed in any one of the preceding claims 1 to 7;
a plurality of word lines extending in parallel in the row direction, respective word lines connecting the control gates of the cells arranged in respective rows; and
a plurality of bit lines extending in parallel in the column direction, respective bit lines connecting the channels of the cells arranged in respective columns.

10. An array according to claim 9 wherein in each column the cells (11-41; 12-42, 13-43, 14-44) are connected in series.

11. An array according to claim 10 wherein the adjacent cells in each column have a common source/drain electrode (54) therebetween.

12. An array according to claim 9 wherein in each column the cells (11-41; 12-42, 13-43, 14-44) are connected in parallel, in each column the sources of the cells being connected to a source line (122,123) and the drains of the cells being connected to a drain line (120,121).

13. An array according to claim 12 wherein in each column the sources are co-extensive and define the source line and the drains are co-extensive and define the drain line.

14. An array according to any of claims 9 to 13 comprising as said plurality of memory cells, cells as claimed in either of claims 4 or 5, wherein in each column said wells (58;98) or said isolated regions (76;108) are co-extensive.

15. An array according to claim 14 wherein said co-extensive wells (58;98) or isolated regions (108) are shunted with a higher concentration impurity semiconductor (63;82; 107) of the same conductivity type.

16. An array according to any of claims 9 to 15 once programmed and having thus the antifuses of selected cells in said low-resistance state, and the antifuses of non-selected cells in said high-resistance state.

17. A method of programming the array of any of claims 9 to 15 whereby the antifuse of a selected cell is changed from said high resistance state to said low resistance state, said method being performed by:-

grounding the sources and the drains of all said cells;
grounding the bit line of the column of cells including the selected cell;
isolating the bit lines of the columns of cells not including the selected cell so that the channels thereof are at a floating potential; and
applying a writing pulse of voltage V_1 to the wordline of the row of cells including the selected cell, whilst the wordlines of the rows of cells not including the selected cell are grounded, the pulse voltage V_1 being related to the breakdown voltage V_{BD} of the control gate insulating layer of the selected cell by the following inequality relationship:

$$V_1 \geq V_{BD} (1 + C_{CG}/C_{FG})$$

18. A memory programming circuit for performing the method of claim 17, said circuit comprising:

the array of any of claims 9 to 15;
a row decoder (10) and a row driver (9), cooperative therewith, for applying the pulse voltage V_1 to the wordline of the row including the selected cell, and for grounding the wordlines of the rows not including the selected cell;
a ground line (-,SW12);
an array of switches (SW5-SW8) interposed between the bit lines of said array and said ground line;
a column decoder (8) arranged to control said array of switches to ground the bit line of the column including the selected cell whilst isolating the bit lines of the columns not including the selected cell;
grounding means (7, SW1-SW4, SW10,SW11) for grounding the sources and drains of all said cells; and
address means (18 to 20) to supply the row and column addresses of the selected cell to said row decoder and said column decoder.

19. A method of reading the array of claim 16 performed by:

setting the bit-line of a selected column at supply voltage V_{CC};
precharging the source and drain of each cell of the selected column to the supply voltage;
applying a reading pulse of voltage V_2 to the wordline of a selected row, wherein V_2 satisfies the following inequalities:
$V_2 > Vth$; $V_2 < Vth\ (1 + C_{FG}/C_{CG})$ where Vth is the threshold value of the transistor having the source, drain, channel and floating gate of the selected cell, grounding the end source or source line of the selected row; and
sensing the voltage on the end drain or drain-line to read the voltage of the cell included in the selected row and selected column.

20. A memory reading circuit for performing the method of claim 19, said circuit comprising:

the array of claim 16;
a row decoder (10) and a row driver (9), cooperative therewith, for grounding the wordlines during precharging, for applying the reading pulse V_2 to the wordline of the selected row, and for grounding the wordlines of the non-selected rows during reading;
a sense line;
a first switch array (SW1-SW4) interposed between said sense line and the end drains or drain lines of said array;
a first column decoder (7) for controlling said first switch array to connect the end drains or draw line of a selected column to said sense line for precharging and for sensing;
a common line connected to the end sources or sense lines;
a channel bias line;
a second switch array (SW5-SW8) interposed between the bit lines of said array and said channel bias line;
a second column decoder (8) for controlling said second switch array to connect the bit line of the selected column to said channel bias line whilst isolating the bit lines of non-selected columns from said bit line; switching means (SW9-SW13) for switching the sense line to the supply voltage V_{CC} for precharging, for isolating the sense line from supply voltage and from ground for sensing, and for grounding the sense line after sensing, for isolating the common line during precharging, and for grounding the common line during reading, for switching the channel bias line to supply voltage V_{CC} for precharging and reading, and for grounding the channel bias line during resetting;
control means (25) for controlling the operation of said switching means in accordance with the method of claim 19; and address means (17-20) to supply the row & column addresses of a selected cell to said row decoder and said first and second column decoders.

21. A memory circuit for performing the method of each of claims 17 and 19, said circuit comprising:

an array according to any of claims 9 to 15;
a row decoder (10), and a row driver (9) cooperative therewith, for applying said voltages to the wordlines of selected rows and for grounding non-selected rows of said array;
a sense line;
a first array of switches (SW1-SW4) interposed between said sense line and the end drain or drain lines of the columns of said array;
a first column decoder (7) for controlling said first array of switches;
a common line connected to the end sources or source lines of said array;
a channel bias line;
a second array of switches (SW5-SW8) interposed between said channel bias line and the bit lines of the array;
a second column decoder for controlling the second array of switches;
address means to supply the row and column addresses of a selected cell to said row decoder and said first and second column decoders;
switching means for isolating said sense line, common line and channel bias line from supply voltage V_{CC} and ground, and for switching them to supply voltage V_{CC} or ground; and
control means for co-ordinating operation of said address means and switching means in accordance with the method of claims 17 and 19.

22. A memory circuit as claimed in claim 21 having said memory array (hereinafter said first memory array);

a second memory array of SRAM, DRAM or flash memory type ;and means for writing and reading data therein;
data input means for supplying same data to be written both in said first memory array and in said second memory array; and
a comparator for comparing the results of reading said first and second memory arrays.

23. A memory circuit according to claim 22 arranged for storing the results of comparison by said comparator in said first memory array.

24. A memory circuit according to either of claims 22 or 23, wherein said memory circuit is a NOR logic gate comprised of transistors which are replicas of the cells of said first memory array.

25. A memory circuit according to any preceding claim 18 to 24 mounted on a card.

26. A memory circuit according to claim 25 having a light receiving element and a light-emitting element arranged for inputting and outputting information.

Patentansprüche

1. Einmal programmierbare Nur-Lese-Speichereinrichtungs(OT-PROM)-Zelle (11) mit:

einer Source (5; 54; 94),
einer Drain (6; 54; 94),
einem Kanal (3; 58; 76; 98) mit zu Source und Drain entgegengesetztem Leitfähigkeitstyp,
einem über dem Kanal angeordneten schwebenden Gate (2; 56; 96),
einer zwischen dem schwebenden Gate und dem Kanal angeordneten Schwebendes-Gate-Isolierschicht (59; 104),
einem über dem schwebenden Gate angeordneten Steuer-Gate (1; 51; 75-91) und
einer zwischen dem Steuer-Gate und dem schwebenden Gate angeordneten Steuer-Gate-Isolierschicht (61; 101 & 102), wobei die Zelle eine Gegensicherung (51, 61, 56; 75, 61, 56; 91, 101, 102, 96) besitzt, die unumkehrbar von einem Zustand hohen Widerstands in einen Zustand niedrigen Widerstands umwandelbar ist,

dadurch gekennzeichnet, daß
die Kapazität C_{FG} zwischen dem schwebenden Gate (2; 56; 96) und dem Kanal (3; 58; 76; 98) größer als die Kapazität C_{CG} zwischen dem Steuer-Gate (1; 51; 75; 91) und dem schwebenden Gate (2; 56; 96) ist und die Gegensicherung (51, 61, 56; 75, 61, 56; 91, 101, 102, 96) aus dem Steuer-Gate (1; 51; 75; 91), der Steuer-Gate-Isolierschicht (61; 101 & 102) und dem schwebenden Gate (2; 56; 96) gebildet ist.

2. Zelle nach Anspruch 1, dadurch gekennzeichnet, daß die Kapazität pro Einheitsbereich zwischen dem Steuer-Gate (1; 51; 75; 91) und dem schwebenden Gate (2; 56; 96) größer als die zwischen dem schwebenden Gate (2; 56; 96) und dem Kanal (3; 58; 76; 98) ist, wodurch der Bereich des schwebenden Gate (2; 56; 96) größer als der überlappende Bereich des Steuer-Gate (1; 51;75; 91) und des schwebenden Gate (2; 56; 96) ist.

3. Zelle nach Anspruch 2, dadurch gekennzeichnet, daß das schwebende Gate zwischen dem Steuer-Gate und dem Kanal angeordnet ist, was keinen Bereich von direkter Überlappung zwischen dem Steuer-Gate und dem Kanal läßt.

4. Zelle nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß
die Source und die Drain in einem Senken(58; 133)-Bereich eines Halbleitersubstrats (60; -) definiert sind, wobei der Kanal ein Teil der Senke ist, der sich zwischen der Source und der Drain erstreckt.

5. Zelle nach einem der Ansprüche 1 bis 3, dadurch gekennzeichnet, daß
die Source (54) und die Drain (54) in einem isolierten Teil (80) einer aktiven Halbleiterschicht (77, 78) auf einem isolierenden Substrat (71) definiert sind, wobei der Kanal ein Teil des isolierten Teils (80) der aktiven Halbleiterschicht ist, der sich zwischen der Source und der Drain erstreckt.

6. Zelle nach einem der Ansprüche 4 oder 5, dadurch gekennzeichnet, daß
die Schwebendes-Gate-Isolierschicht (104; 113) und das schwebende Gate (96; 112) sich vertikal abwärts auf jeder Seite des Kanals (98; 108) erstrecken, um die Kapazität dazwischen zu erhöhen.

7. Zelle nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß
die Schwebendes-Gate-Isolierschicht aus Siliziumoxynitrid (SiON) besteht und das schwebende Gate aus dotiertem polykristallinen Silizium (Poly-Si) besteht.

8. Zelle nach einem der vorhergehenden Ansprüche, die einmal programmiert ist und somit die Gegensicherung in dem Zustand niedrigen Widerstands besitzt.

9. OT-PROM-Speichereinrichtungsfeld mit:

einer Vielzahl von in Reihen und Spalten angeordneten Speichereinrichtungszellen (11-44), wobei jede Zelle eine Zelle nach einem der vorhergehenden Ansprüche 1 bis 7 ist,
einer Vielzahl von sich parallel in der Reihenrichtung erstreckenden Wortleitungen, wobei jeweilige Wortleitungen die Steuer-Gates der in jeweiligen Reihen angeordnet Zellen verbinden, und
einer Vielzahl von sich parallel in der Spaltenrichtung erstreckenden Bitleitungen, wobei jeweilige Bitleitungen die Kanäle der in jeweiligen Spalten angeordneten Zellen verbinden.

10. Feld nach Anspruch 9, dadurch gekennzeichnet, daß in jeder Spalte die Zellen (11-41; 12-42, 13-43, 14-44) in Reihe verbunden sind.

11. Feld nach Anspruch 10, dadurch gekennzeichnet, daß die benachbarten Zellen in jeder Spalte eine gemeinsame Source/Drain-Elektrode (54) dazwi-

schen besitzen.

12. Feld nach Anspruch 9, dadurch gekennzeichnet, daß in jeder Spalte die Zellen (11-41; 12-42, 13-43, 14-44) parallel verbunden sind, wobei in jeder Spalte die Sources der Zellen mit einer Source-Leitung (122, 123) und die Drains der Zellen mit einer Drain-Leitung (120, 121) verbunden sind.

13. Feld nach Anspruch 12, dadurch gekennzeichnet, daß in jeder Spalte die Sources sich gemeinsam erstrecken und die Source-Leitung definieren und die Drains sich gemeinsam erstrecken und die Drain-Leitung definieren.

14. Feld nach einem der Ansprüche 9 bis 13, mit als die Vielzahl von Speichereinrichtungszellen Zellen nach einem der Ansprüche 4 oder 5, wobei sich in jeder Spalte die Senken (58; 98) oder die isolierten Bereiche (76; 108) gemeinsam erstrecken.

15. Feld nach Anspruch 14, dadurch gekennzeichnet, daß die sich gemeinsam erstreckenden Senken (58; 98) oder isolierten Bereiche (108) einen Nebenschluß mit einem Halbleiter (63; 82; 107) mit einer höheren Konzentration Verunreinigungen desselben Leitfähigkeitstyps bilden.

16. Feld nach einem der Ansprüche 9 bis 15, das einmal programmiert ist und somit die Gegensicherungen von ausgewählten Zellen in dem Zustand niedrigen Widerstands hat und die Gegensicherungen von nicht ausgewählten Zellen in dem Zustand hohen Widerstands hat.

17. Verfahren zum Programmieren des Feld nach einem der Ansprüche 9 bis 15, wobei die Gegensicherung einer ausgewählten Zelle von einem Zustand hohen Widerstands in einen Zustand niedrigen Widerstands verändert wird, mit den Schritten:

    auf Masse Legen der Sources und Drains aller Zellen, auf Masse Legen der Bitleitung der Spalte von Zellen, die die ausgewählte Zelle enthält,
    Isolieren der Bitleitungen der Spalten von Zellen, die die ausgewählte Zelle nicht enthalten, so daß deren Kanäle auf einem schwebenden Potential sind, und
    Anlegen eines Schreibimpulses einer Spannung V_1 an die Wortleitung der Reihe von Zellen, die die ausgewählte Zelle einschließt, während die Wortleitungen der Reihen von Zellen, die die ausgewählte Zelle nicht enthalten, auf Masse gelegt sind, wobei die Impulsspannung V_1 sich auf die Durchbruchspannung V_{BD} der Steuer-Gate-Isolierschicht der ausgewählten Zelle durch die folgende Ungleichungsbeziehung bezieht:

$$V_1 \geq V_{BD} (1 + C_{CG}/C_{FG})$$

18. Speichereinrichtungsprogrammierungsschaltung zur Durchführung des Verfahrens nach Anspruch 17, mit:

    dem Feld nach einem der Ansprüche 9 bis 15,
    einer Reihendekodiereinrichtung (10) und einer Reihenansteuereinrichtung (9), die damit zusammenwirkt, zum Anlegen der Impulsspannung V_1 an die Wortleitung der Reihe, die die ausgewählte Zelle enthält, und zum auf Masse Legen der Wortleitungen der Reihen, die die ausgewählte Zelle nicht einschließen,
    einer Masseleitung (-, SW12),
    einem Feld von Schaltern (SW5-SW8), das zwischen den Bitleitungen des Felds und der Masseleitung angeordnet ist,
    einer Spaltendekodiereinrichtung (8), die zur Steuerung des Felds von Schaltern angeordnet ist, um die Bitleitung der Spalte, die die ausgewählte Zelle enthält, auf Masse zu legen, während die Bitleitungen der Spalten, die die ausgewählte Zelle nicht enthalten, isoliert sind,
    einer Auf-Masse-Legeeinrichtung (7, SW1-SW4, SW10, SW11) zum auf Masse Legen der Sources und Drains aller Zellen und einer Adressierungseirnichtung (18 bis 20) zur Zuführung der Reihen- und Spaltenadressen der ausgewählten Zelle zu der Reihendekodiereinrichtung und der Spaltendekodiereinrichtung.

19. Verfahren zum Lesen des Felds nach Anspruch 16, mit den Schritten:

    Setzen der Bitleitung einer ausgewählten Spalte auf eine Versorgungsspannung V_{CC},
    Vorladen der Source und Drain jeder Zelle der ausgewählten Spalte auf die Versorgungsspannung,
    Anlegen eines Leseimpulses mit einer Spannung V_2 an die Wortleitung einer ausgewählten Reihe, wobei V_2 die folgenden Ungleichungen erfüllt:

$$V_2 > Vth; V_2 < Vth (1 + C_{FG}/C_{CG})$$

    wobei Vth der Schwellenwert des Transistors ist, der die Source, Drain, Kanal und das schwebende Gate der ausgewählten Zelle besitzt,
    auf Masse Legen der End-Source oder Source-Leitung der ausgewählten Reihe und

Erfassen der Spannung an der End-Drain oder Drainleitung, um die Spannung der Zelle zu lesen, die in der ausgewählten Reihe und der ausgewählten Spalte enthalten ist.

20. Speichereinrichtungsleseschaltung zur Durchführung des Verfahrens nach Anspruch 19, mit:

dem Feld nach Anspruch 16,
einer Reihendekodiereinrichtung (10) und einer Reihenansteuereinrichtung (9), die damit zusammenwirkt, zum auf Masse Legen der Wortleitungen während des Vorladens, zum Anlegen des Leseimpulses V_2 an die Wortleitung der ausgewählten Reihe und zum auf Masse Legen der Wortleitungen der nicht ausgewählten Reihen während des Lesens,
einer Erfassungsleitung,
einem ersten Schalterfeld (SW1-SW4), das zwischen der Erfassungsleitung und den End-Drains oder Drain-Leitungen des Felds angeordnet ist,
einer ersten Spaltendekodiereinrichtung (7) zur Steuerung des ersten Schalterfelds, um die End-Drains oder Drain-leitungen einer ausgewählten Spalte mit der Erfassungsleitung zum Vorladen und Erfassen zu verbinden,
einer gemeinsamen Leitung, die mit den End-Sources oder Erfassungsleitungen verbunden ist,
einer Kanalvorspannungsleitung,
einem zweiten Schalterfeld (SW5-SW8), das zwischen den Bitleitungen des Felds und der Kanalvorspannungsleitung angeordnet ist,
einer zweiten Spaltendekodiereinrichtung (8) zur Steuerung des zweiten Schalterfelds, um die Bitleitung der ausgewählten Spalte mit der Kanalvorspannungsleitung zu verbinden, während die Bitleitungen der nicht ausgewählten Spalten von der Bitleitung isoliert sind,
einer Schalteinrichtung (SW9-SW13) zum Schalten der Erfassungleitung auf die Versorgungsspannung Vcc zur Vorladung, zum Isolieren der Erfassungsleitung von der Versorgungsspannung und von Masse zur Erfassung und zum auf Masse legen der Erfassungsleitung nach der Erfassung, zur Isolierung der gemeinsamen Leitung während des Vorladens und zum auf Masse Legen der gemeinsamen Leitung während des Lesens, zum Schalten der Kanalvorspannungsleitung auf die Versorgungsspannung V_{CC} zur Vorladung und zum Lesen und zum auf Masse Legen der Kanalvorspannungsleitung während eines Rücksetzens,
einer Steuereinrichtung (25) zur Steuerung der Funktion der Schalteinrichtung entsprechend dem Verfahren nach Anspruch 19,
und einer Adresseinrichtung (17-20) zur Zuführung der Reihen- und Spaltenadressen einer ausgewählten Zelle zur Reihendekodiereinrichtung und den ersten und zweiten Spaltendekodiereinrichtungen.

21. Speichereinrichtungsschaltung zur Durchführung des Verfahrens nach jedem der Ansprüche 17 und 19, mit:

einem Feld nach einer der Ansprüche 9 bis 15,
einer Reihendekodiereinrichtung (10) und einer Reihenansteuereinrichtung (9), die damit zusammenwirkt, zum Anlegen der Spannungen an die Wortleitungen von ausgewählten Reihen und zum auf Masse Legen von nicht ausgewählten Reihen des Felds,
einer Erfassungsleitung,
einem ersten Feld von Schaltern (SW1-SW4), das zwischen der Erfassungsleitung und dem End-Drain oder Drain-Leitungen der Spalten des Felds angeordnet ist,
einer ersten Spaltendekodiereinrichtung (7) zur Steuerung des ersten Felds von Schaltern,
einer gemeinsamen Leitung, die mit den End-Sources oder Source-Leitungen des Felds verbunden ist,
einer Kanalvorspannungsleitung,
einem zweiten Feld von Schaltern (SW5-SW8), das zwischen der Kanalvorspannungsleitung und den Bitleitungen des Felds angeordnet ist,
einer zweiten Spaltendekodiereinrichtung zur Steuerung des zweiten Felds von Schaltern,
einer Adresseinrichtung zur Zuführung der Reihen- und Spaltenadressen einer ausgewählten Zelle zur Reihendekodiereinrichtung und den ersten und zweiten Spaltendekodiereinrichtungen,
einer Schalteinrichtung zur Isolierung der Erfassungsleitung, der gemeinsamen Leitung und der Kanalvorspannungsleitung von der Versorgungsspannung V_{CC} und Masse und zum Schalten von ihnen zur Versorgungsspannung V_{CC} oder Masse und
einer Steuereinrichtung zur Koordination der Funktion der Adresseinrichtung und der Schalteinrichtung entsprechend dem Verfahren nach den Ansprüchen 17 und 19.

22. Speichereinrichtungsschaltung nach Anspruch 21 mit dem Speichereinrichtungsfeld (im folgenden dem ersten Speichereinrichtungsfeld),

einem zweiten Speichereinrichtungsfeld vom SRAM, DRAM oder Flash-Speichereinrichtungs-Typ,
einer Einrichtung zum Schreiben und Lesen von Daten darin, einer Dateneingabeeinrich-

tung zur Zufuhr derselben Daten, damit sie sowohl in das erste Speichereinrichtungsfeld als auch in das zweite Speichereinrichtungsfeld geschrieben werden, und
einer Vergleichseinrichtung zum Vergleich der Ergebnisse eines Lesens der ersten und zweiten Speichereinrichtungsfelder.

23. Speichereinrichtungsschaltung nach Anspruch 22, die zur Speicherung der Ergebnisse eines Vergleichs durch die Vergleichseinrichtung in dem ersten Speichereinrichtungsfeld ausgebildet ist.

24. Speichereinrichtungsschaltung nach einem der Ansprüche 22 oder 23, dadurch gekennzeichnet, daß die Speichereinrichtungsschaltung ein Nicht-Oder-Logikgatter ist, das aus Transistoren besteht, die Kopie der Zellen des ersten Speichereinrichtungsfelds sind.

25. Speichereinrichtungsschaltung nach einem der vorhergehenden Ansprüche 18 bis 24, die auf einer Karte montiert ist.

26. Speichereinrichtungsschaltung nach Anspruch 25 mit einem Lichtempfangselement und einem Lichtemissionselement, die zur Eingabe und Ausgabe von Informationen angeordnet sind.

Revendications

1. Cellule (11) de mémoire morte programmable une seule fois (OT-PROM) comprenant :

une source (5; 54; 94);
un drain (6; 54; 94);
un canal (3; 58; 76; 98) d'un type de conductivité opposé à la source et au drain;
une grille flottante (2; 56; 96) placée au-dessus du canal;
une couche d'isolant de grille flottante (59; 104) disposée entre la grille flottante et le canal;
une grille de commande (1; 51; 75-91) placée au-dessus de la grille flottante; et
une couche d'isolant de grille de commande (61; 101 & 102) disposée entre la grille de commande et la grille flottante;
cette cellule ayant un anti-fusible (51, 61, 56; 75, 61, 56; 91, 101, 102, 96) qui peut être converti de façon irréversible d'un état à haute résistance à un état à faible résistance;

caractérisé en ce que :
la capacité C_{FG} entre la grille flottante (2; 56; 96) et le canal (3; 58; 76; 98) est supérieure à la capacité C_{CG} entre la grille de commande (1; 51; 75; 91) et la grille flottante (2; 56; 96) et l'anti-fusible (51, 61, 56; 75, 61, 56; 91, 101, 102, 96) est formé par la grille de commande (1; 51; 75; 91), la couche d'isolant de grille de commande (61; 101 & 102), et la grille flottante (2; 56; 96) .

2. Cellule selon la revendication 1, dans laquelle la capacité par unité d'aire entre la grille de commande (1; 51; 75; 91) et la grille flottante (2; 56; 96) est supérieure à celle entre la grille flottante (2; 56; 96) et le canal (3; 58; 76; 98), l'aire de la grille flottante (2; 56; 96) étant donc supérieure à l'aire de recouvrement de la grille de commande (1; 51; 75; 91) et de la grille flottante (2; 56; 96).

3. Cellule selon la revendication 2, dans laquelle la grille flottante est interposée entre la grille de commande et le canal en ne laissant aucune zone de recouvrement direct entre la grille de commande et le canal.

4. Cellule selon l'une quelconque des revendications 1 à 3, dans laquelle la source et le drain sont définis dans une région de caisson (58; 133) d'un substrat semiconducteur (60; -), le canal faisant partie du caisson et s'étendant entre la source et le drain.

5. Cellule selon l'une quelconque des revendications 1 à 3, dans laquelle la source (54) et le drain (54) sont définis dans une partie isolée (80) d'une couche active semiconductrice (77, 78) sur un substrat semiconducteur (71), le canal faisant partie de la partie isolée (80) de la couche active semiconductrice et s'étendant entre la source et le drain.

6. Cellule selon l'une quelconque des revendications 4 ou 5, dans laquelle la couche isolante de grille flottante (104; 113) et la grille flottante (96; 112) s'étendent verticalement vers le bas de chaque côté du canal (98; 108) pour augmenter la capacité entre elles.

7. Cellule selon l'une quelconque des revendications précédentes, dans laquelle la couche isolante de grille flottante est en oxynitrure de silicium (SiON) et la grille flottante est en silicium polycristallin dopé (poly-Si).

8. Cellule selon l'une quelconque des revendications précédentes, ayant été programmée une fois et ayant donc l'anti-fusible dans l'état à faible résistance.

9. Réseau de mémoire OT-PROM comprenant :

une pluralité de cellules de mémoire (11-44) disposées en rangées et en colonnes, chaque cellule étant une cellule revendiquée dans l'une quelconque des revendications 1 à 7 précéden-

tes;
une pluralité de lignes de mot s'étendant en parallèle dans la direction des rangées, des lignes de mot respectifs connectant les grilles de commande des cellules disposées dans des rangées respectives; et
une pluralité de lignes de bit s'étendant en parallèle dans la direction des colonnes, des lignes de bit respectifs connectant les canaux des cellules disposées dans des colonnes respectives.

10. Réseau selon la revendication 9, dans lequel dans chaque colonne les cellules (11-41; 12-42; 13-43; 14-44) sont connectées en série.

11. Réseau selon la revendication 10, dans lequel les cellules adjacentes dans chaque colonne ont une électrode de source/drain commune (54) entre elles.

12. Réseau selon la revendication 9, dans lequel dans chaque colonne les cellules (11-41; 12-42; 13-43; 14-44) sont connectées en parallèle, dans chaque colonne les sources des cellules étant connectées à une ligne de source (122, 123) et les drains des cellules étant connectés à une ligne de drain (120, 121).

13. Réseau selon la revendication 12, dans lequel dans chaque colonne les sources s'étendent de façon contiguë et définissent la ligne de source et les drains s'étendent de façon contiguë et définissent la ligne de drain.

14. Réseau selon l'une quelconque des revendications 9 à 13, comprenant pour la pluralité de cellules de mémoire, des cellules telles que celles revendiquées dans l'une ou l'autre des revendications 4 ou 5, dans lequel dans chaque colonne les caissons (58; 98) ou les régions isolées (76; 108) sont contigus.

15. Réseau selon la revendication 14, dans lequel les caissons (58; 98) ou les régions isolées (108) contigus sont shuntés par un semiconducteur (63; 82; 107) à concentration en impuretés supérieure, du même type de conductivité.

16. Réseau selon l'une quelconque des revendications 9 à 15, ayant été programmé et ayant donc les anti-fusibles de cellules sélectionnées dans l'état à faible résistance, et les anti-fusibles de cellules non sélectionnées dans l'état à haute résistance.

17. Procédé de programmation du réseau de l'une quelconque des revendications 9 à 15, par lequel l'anti-fusible d'une cellule sélectionnée est changé de l'état à haute résistance à l'état à faible résistance, ce procédé étant accompli par :

la mise à la masse des sources et des drains de toutes les cellules;
la mise à la masse de la ligne de bit de la colonne de cellules comprenant la cellule sélectionnée;
l'isolation des lignes de bit des colonnes de cellules ne comprenant pas la cellule sélectionnée, de façon que leurs canaux soient à un potentiel flottant;
l'application d'une impulsion d'écriture de tension V_1 à la ligne de mot de la rangée de cellules comprenant la cellule sélectionnée, tandis que les lignes de mot des rangées de cellules ne comprenant pas la cellule sélectionnée sont mis à la masse, la tension d'impulsion V_1 étant liée à la tension de claquage V_{BD} de la couche d'isolant de grille de commande de la cellule sélectionnée par la relation d'inégalité suivante :

$$V_1 \geq V_{BD} (1 + C_{CG}/C_{FG})$$

18. Circuit de programmation de mémoire pour accomplir le procédé de la revendication 17, ce circuit comprenant :

le réseau de l'une quelconque des revendications 9 à 15;
un décodeur de rangée (10) et un circuit d'attaque de rangée (9), coopérant avec celui-ci, pour appliquer la tension d'impulsion V_1 à la ligne de mot de la rangée comprenant la cellule sélectionnée, et pour mettre à la masse les lignes de mot des rangées ne comprenant pas la cellule sélectionnée;
une ligne de masse (-, SW12);
un réseau d'éléments de commutation (SW5-SW8) interposés entre les lignes de bit du réseau et la ligne de masse;
un décodeur de colonne (8) adapté pour commander le réseau d'éléments de commutation pour mettre à la masse la ligne de bit de la colonne comprenant la cellule sélectionnée, tout en isolant les lignes de bit des colonnes ne comprenant pas la cellule sélectionnée;
des moyens de mise à la masse (7, SW1-SW4, SW10, SW11) pour mettre à la masse les sources et les drains de toutes les cellules; et
des moyens d'adressage (18 à 20) pour fournir les adresses de rangée et de colonne de la cellule sélectionnée au décodeur de rangée et au décodeur de colonne.

19. Procédé de lecture du réseau de la revendication 16, accompli par :

la fixation de la ligne de bit d'une colonne sélectionnée à la tension d'alimentation V_{CC};
la précharge à la tension d'alimentation de la source et du drain de chaque cellule de la colonne sélectionnée;
l'application d'une impulsion de lecture de tension V_2 à la ligne de mot d'une rangée sélectionnée, V_2, vérifiant les inégalités suivantes : $V_2 > Vth$; $V_2 < Vth\ (1 + C_{FG}/C_{CG})$ en désignant par Vth la valeur de seuil du transistor ayant la source, le drain, le canal et la grille flottante de la cellule sélectionnée, mettant à la masse la source d'extrémité ou la ligne de source de la rangée sélectionnée; et
la détection de la tension sur le drain d'extrémité ou la ligne de drain, pour lire la tension de la cellule incluse dans la rangée sélectionnée et la colonne sélectionnée.

20. Circuit de lecture de mémoire pour accomplir le procédé de la revendication 19, ce circuit comprenant :

le réseau de la revendication 16;
un décodeur de rangée (10) et un circuit d'attaque de rangée (9), coopérant avec celui-ci, pour mettre à la masse les lignes de mot pendant la précharge, pour appliquer l'impulsion de lecture V_2 à la ligne de mot de la rangée sélectionnée, et pour mettre à la masse les lignes de mot des rangées non sélectionnées pendant la lecture;
une ligne de détection;
un premier réseau d'éléments de commutation (SW1-SW4) interposés entre la ligne de détection et les drains d'extrémité ou les lignes de drain du réseau;
un premier décodeur de colonne (7) pour commander le premier réseau d'éléments de commutation de façon à connecter les drains d'extrémité ou la ligne de drain d'une colonne sélectionnée à la ligne de détection, pour la précharge et pour la détection;
une ligne commune connectée aux sources d'extrémité ou aux lignes de détection;
une ligne de polarisation de canal;
un second réseau d'éléments de commutation (SW5-SW8) interposés entre les lignes de bit du réseau et la ligne de polarisation de canal;
un second décodeur de colonne (8) pour commander le second réseau d'éléments de commutation de façon à connecter la ligne de bit de la colonne sélectionnée à la ligne de polarisation de canal, tout en isolant de ladite ligne de bit les lignes de bit de colonnes non sélectionnées; des moyens de commutation (SW9-SW13) pour commuter la ligne de détection à la tension d'alimentation V_{CC} pour la précharge, pour isoler la ligne de détection de la tension d'alimentation et de la masse pour la détection, et pour mettre à la masse la ligne de détection après détection, pour isoler la ligne commune pendant la précharge, et pour mettre à la masse la ligne commune pendant la lecture, pour commuter la ligne de polarisation de canal à la tension V_{CC} pour la précharge et la lecture, et pour mettre à la masse la ligne de polarisation de canal pendant la restauration;
des moyens de commande (25) pour commander le fonctionnement des moyens de commutation conformément au procédé de la revendication 19; et des moyens d'adressage (17-20) pour fournir les adresses de rangée et de colonne d'une cellule sélectionnée au décodeur de rangée et aux premier et second décodeurs de colonne.

21. Circuit de mémoire pour accomplir le procédé de chacune des revendications 17 et 19, ce circuit comprenant :

un réseau selon l'une quelconque des revendications 9 à 15;
un décodeur de rangée (10), et un circuit d'attaque de rangée (9) coopérant avec celui-ci, pour appliquer lesdites tensions aux lignes de mot de rangées sélectionnées et pour mettre à la masse des rangées non sélectionnées du réseau;
une ligne de détection;
un premier réseau d'éléments de commutation (SW1-SW4) interposés entre la ligne de détection et le drain d'extrémité ou des lignes de drain des colonnes du réseau;
un premier décodeur de colonne (7) pour commander le premier réseau d'éléments de commutation;
une ligne commune connectée aux sources d'extrémité ou aux lignes de source du réseau;
une ligne de polarisation de canal;
un second réseau d'éléments de commutation (SW5-SW8) interposés entre la ligne de polarisation de canal et les lignes de bit du réseau;
un second décodeur de colonne pour commander le second réseau d'éléments de commutation;
des moyens d'adressage pour fournir les adresses de rangée et de colonne d'une cellule sélectionnie au décodeur de rangée et aux premier et second décodeurs de colonne;
des moyens de commutation pour isoler de la tension d'alimentation V_{CC} et de la masse la ligne de détection, la ligne commune et la ligne de polarisation de canal, et pour les commuter à la tension d'alimentation V_{CC} ou à la masse; et
des moyens de commande pour coordonner le

fonctionnement des moyens d'adressage et des moyens de commutation conformément au procédé des revendications 17 et 19.

22. Circuit de mémoire selon la revendication 21 ayant ledit réseau de mémoire (appelé ci-après le premier réseau de mémoire) ;

un second réseau de mémoire du type mémoire vive statique (ou SRAM), mémoire vive dynamique (ou DRAM) ou mémoire flash; et des moyens pour écrire et lire des données dans celui-ci;
des moyens d'entrée de données pour appliquer les mêmes données à écrire à la fois dans le premier réseau de mémoire et dans le second réseau de mémoire; et
un comparateur pour comparer les résultats de lecture des premier et second réseaux de mémoire.

23. Circuit de mémoire selon la revendication 22, adapté pour stocker dans le premier réseau de mémoire les résultats de la comparaison par le comparateur.

24. Circuit de mémoire selon l'une quelconque des revendications 22 ou 23, dans lequel le circuit de mémoire est une porte logique NON-OU constituée par des transistors qui sont des répliques des cellules du premier réseau de mémoire.

25. Circuit de mémoire selon l'une quelconque des revendications 18 à 24 précédentes, monté sur une carte.

26. Circuit de mémoire selon la revendication 25 ayant un élément de réception de lumière et un élément d'émission de lumière adaptés pour l'entrée et la sortie d'information.

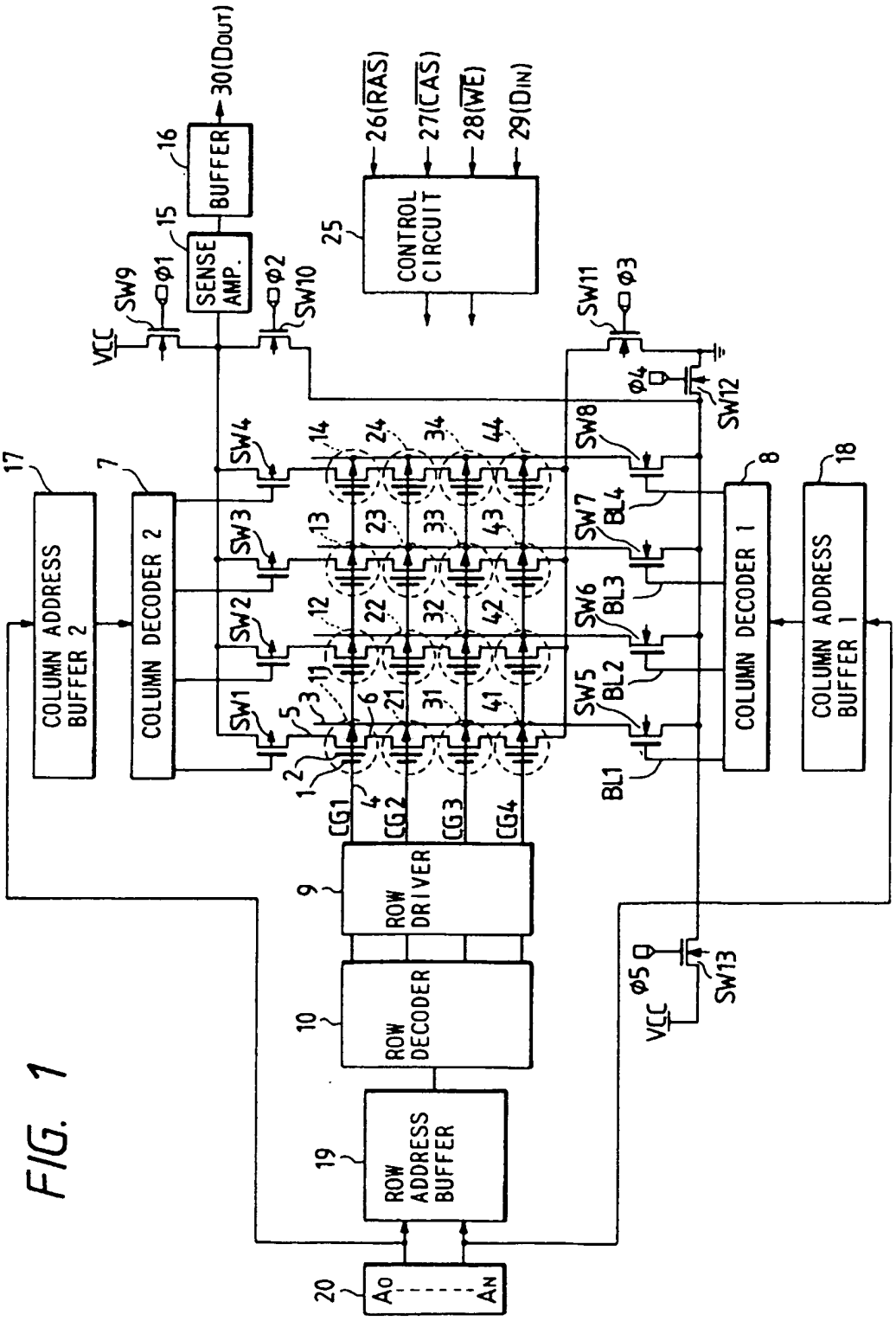
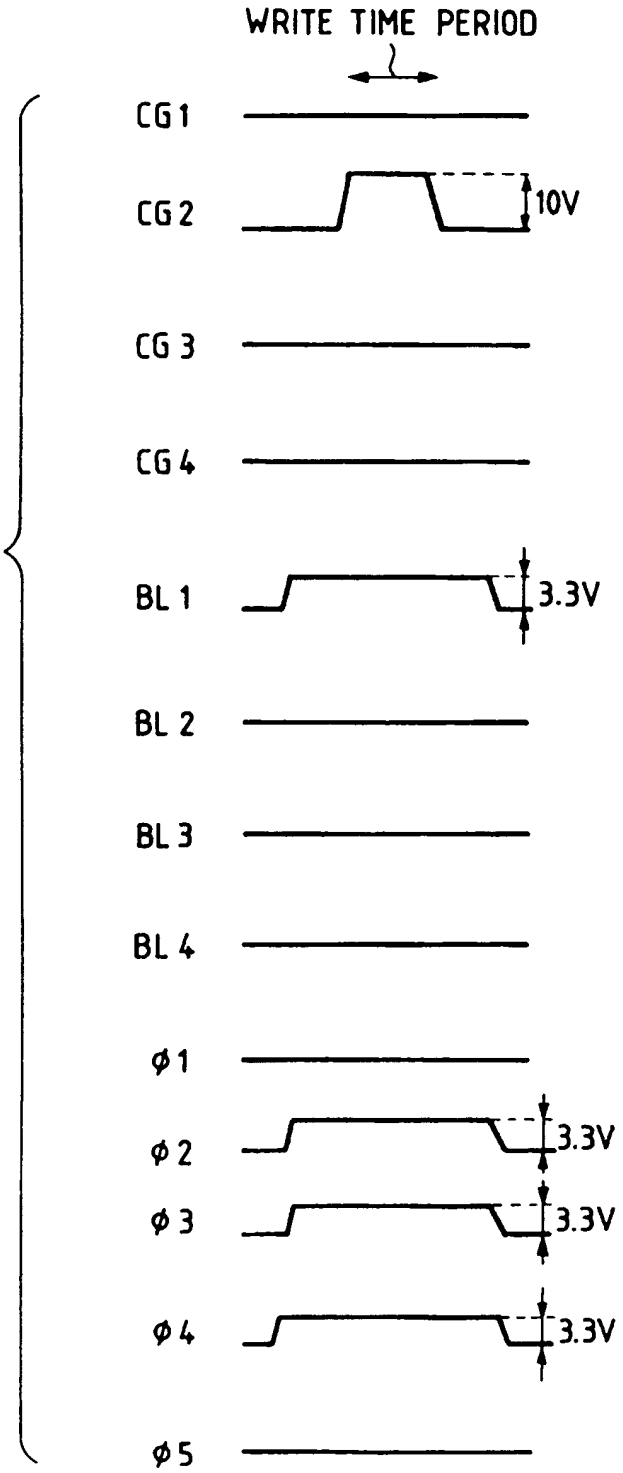

30(DOUT)
16
BUFFER
15
SENSE AMP.
φ1
φ2
SW9
SW10
VCC
26(RAS)
27(CAS)
28(WE)
29(DIN)
25
CONTROL CIRCUIT
SW11
φ3
φ4
SW12
17
COLUMN ADDRESS BUFFER 2
7
COLUMN DECODER 2
SW4
SW3
SW2
SW1
SW8
SW7
SW6
SW5
BL4
BL3
BL2
BL1
8
COLUMN DECODER 1
18
COLUMN ADDRESS BUFFER 1
CG1
CG2
CG3
CG4
9
ROW DRIVER
10
ROW DECODER
19
ROW ADDRESS BUFFER
20
A0
AN
φ5
SW13
VCC

FIG. 1

FIG. 2


WRITE TIME PERIOD
CG1
CG2
10V
CG3
CG4
BL1
3.3V
BL2
BL3
BL4
φ1
φ2
3.3V
φ3
3.3V
φ4
3.3V
φ5

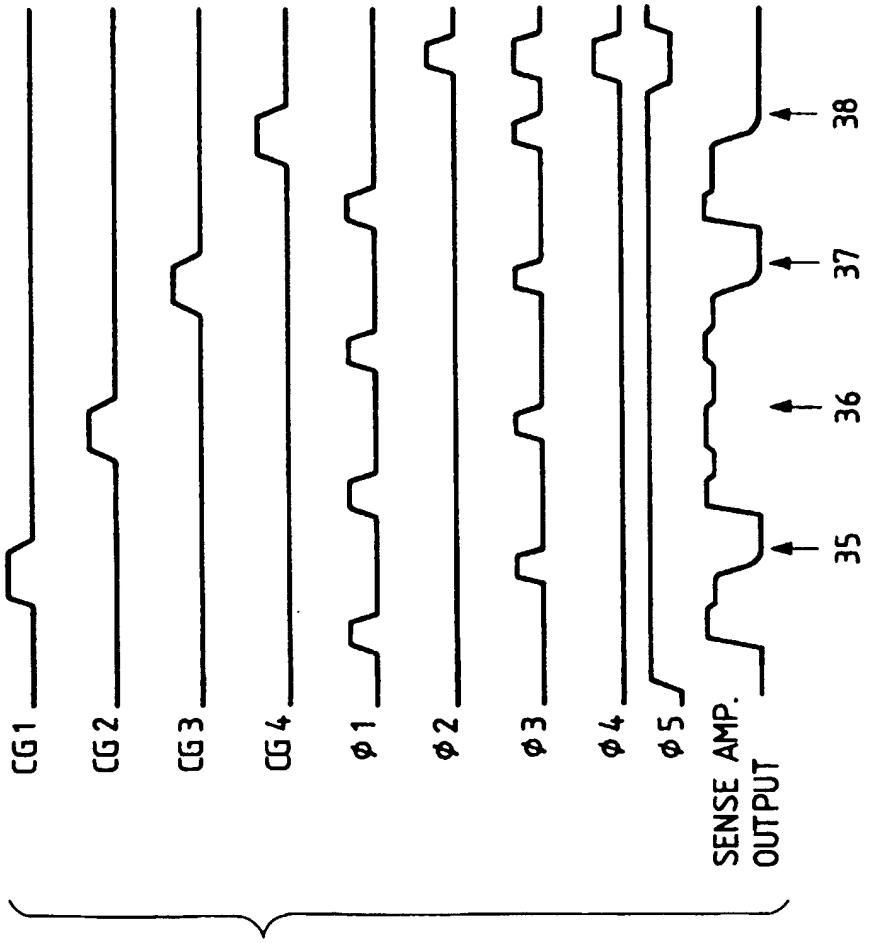


FIG. 3

FIG. 4

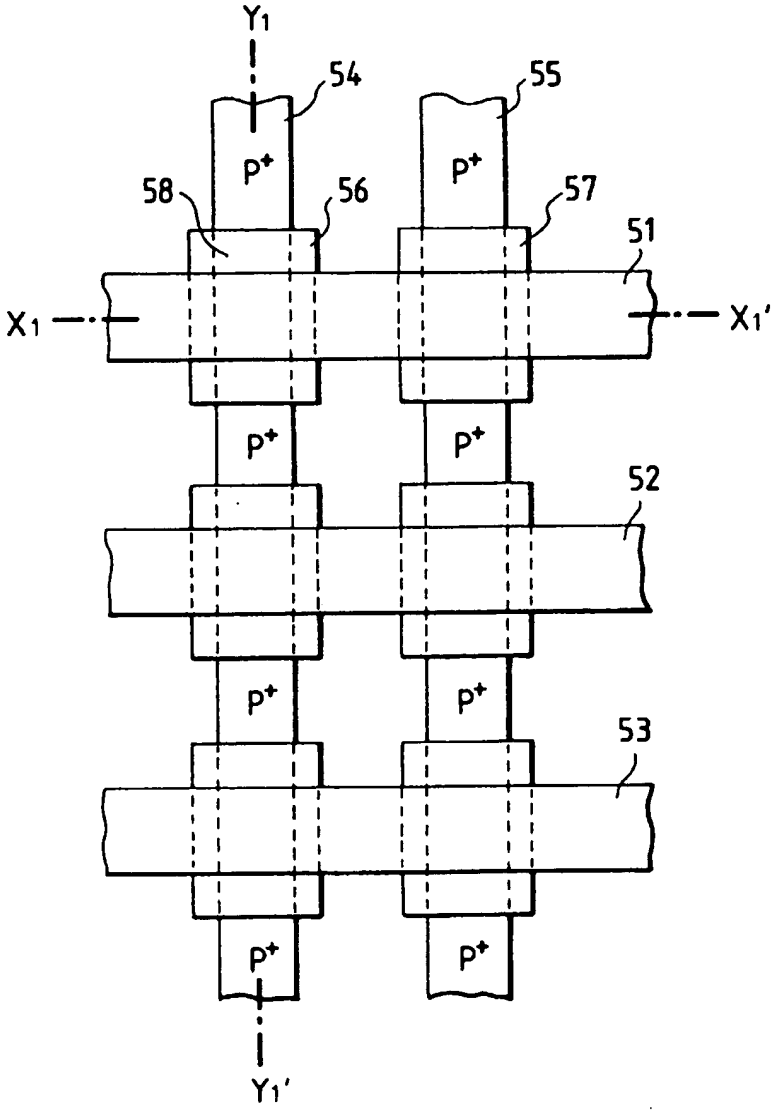


FIG. 5A

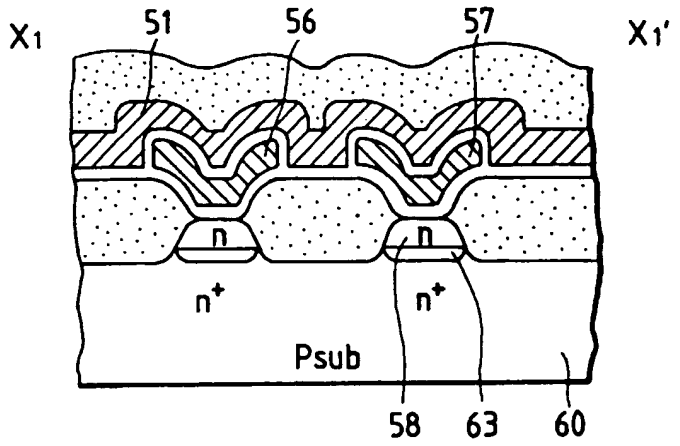

X1
51
56
57
X1'
n
n
n+
n+
Psub
58
63
60

FIG. 5B

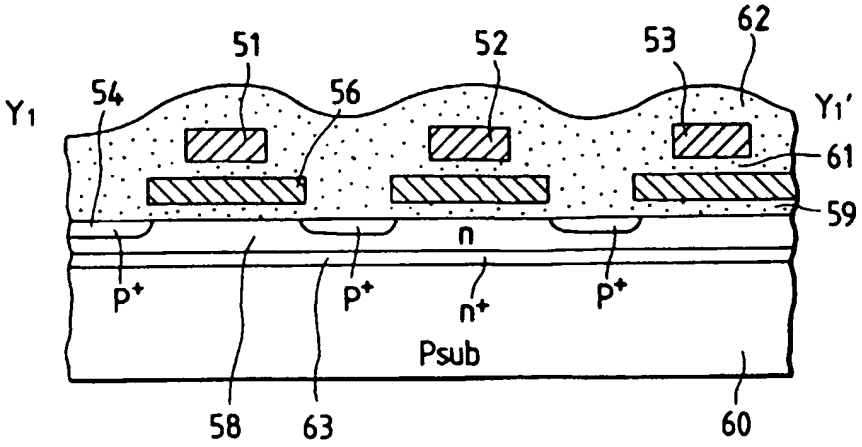

Y1
54
51
56
52
53
62
Y1'
61
59
n
P+
P+
n+
P+
Psub
58
63
60

FIG. 6A

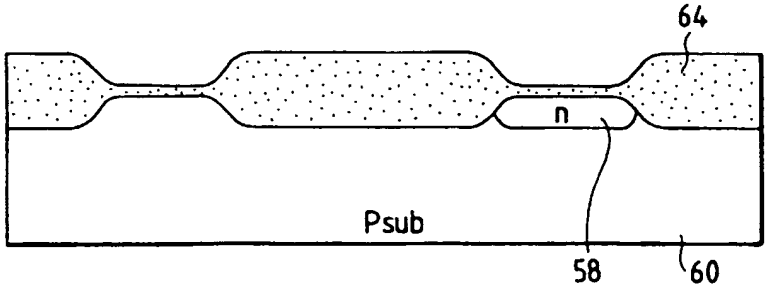


FIG. 6B

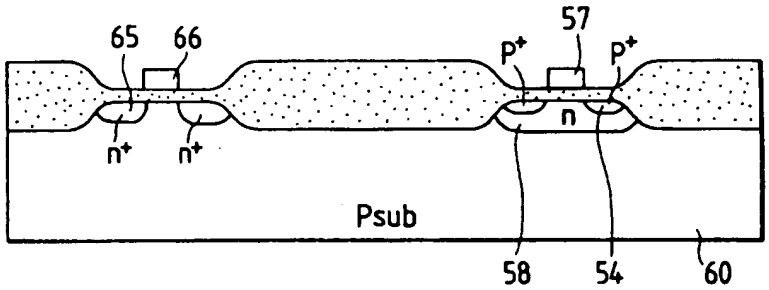


FIG. 6C

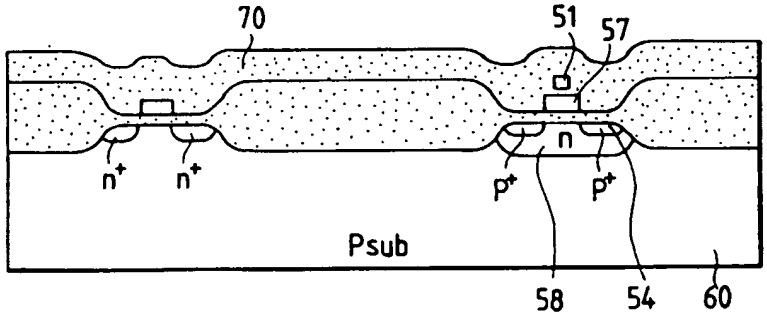


FIG. 6D

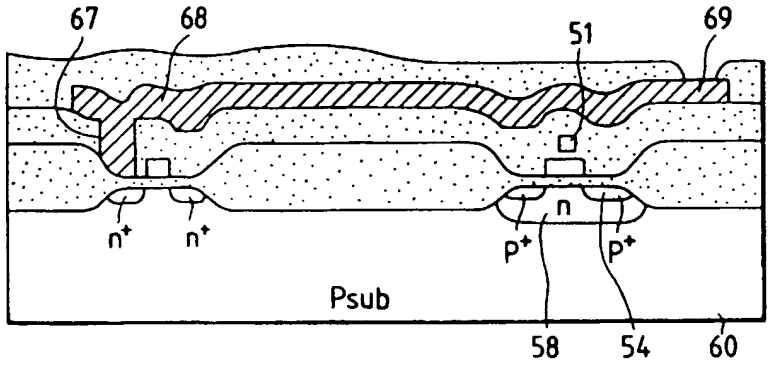


FIG. 7A

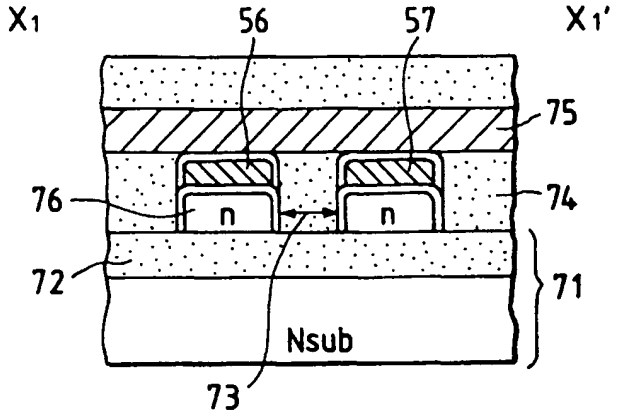

X1
56
57
X1'
75
76
n
n
74
72
71
Nsub
73

FIG. 7B

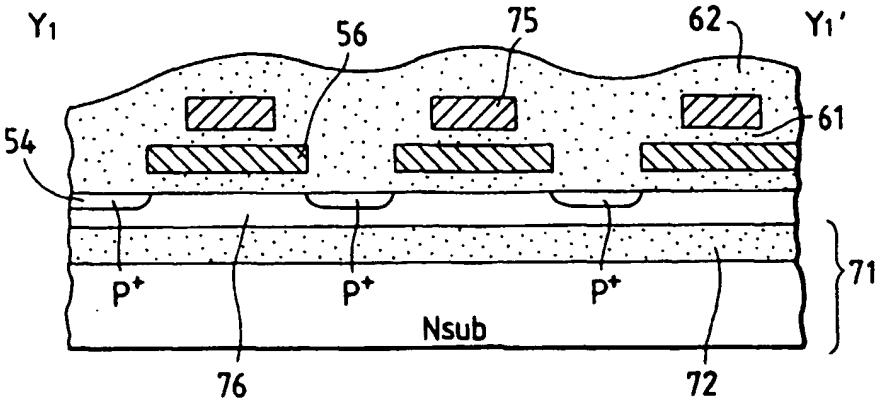

Y1
56
75
62
Y1'
61
54
P+
P+
P+
71
Nsub
76
72

FIG. 8A

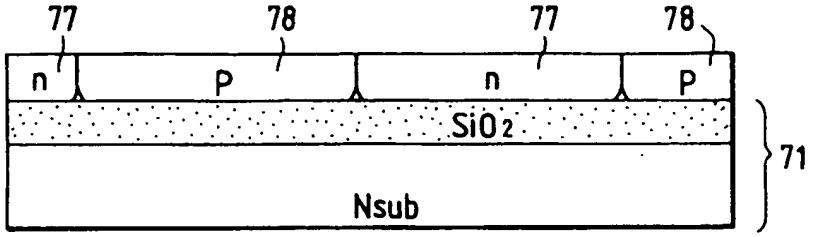


FIG. 8B

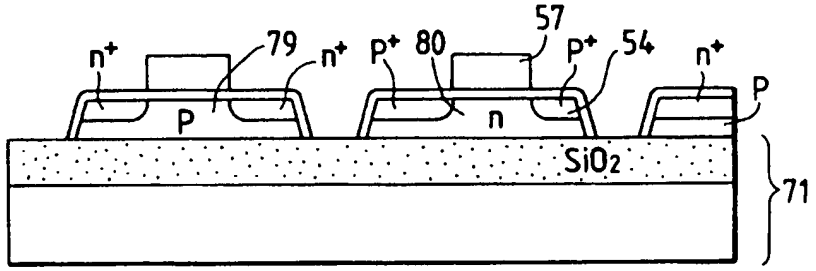


FIG. 8C

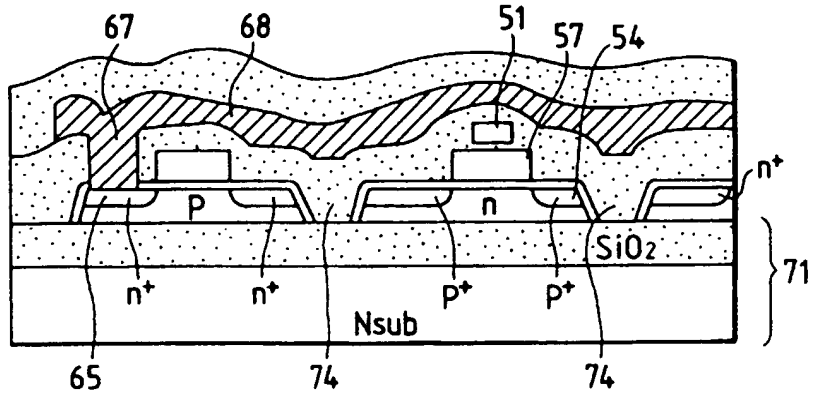


FIG. 9A

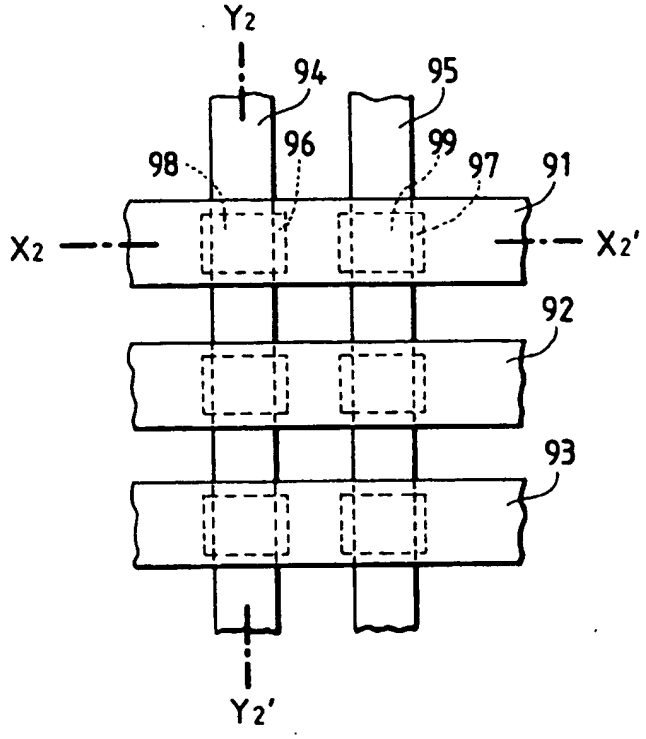


FIG. 9B

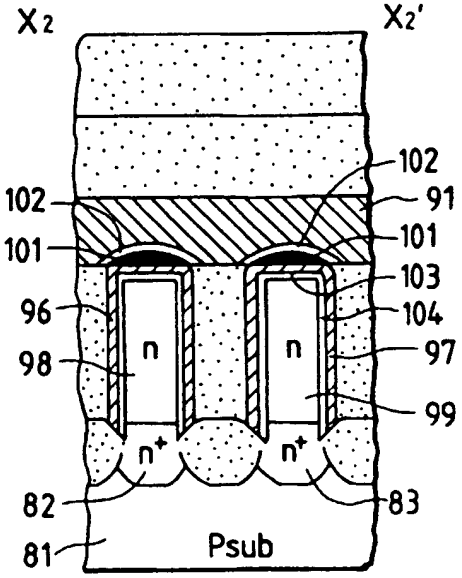


FIG. 9C

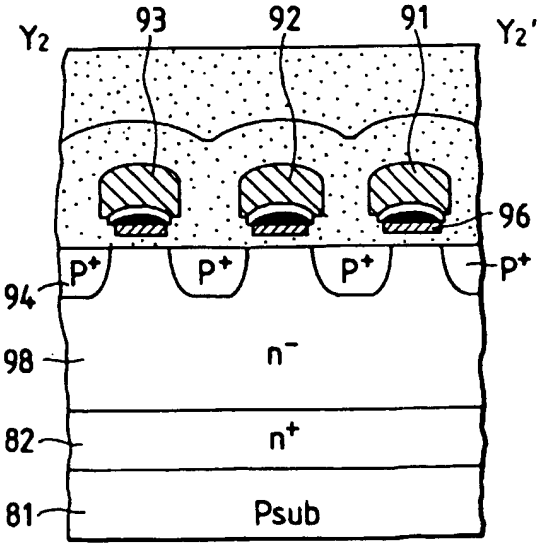


FIG. 10

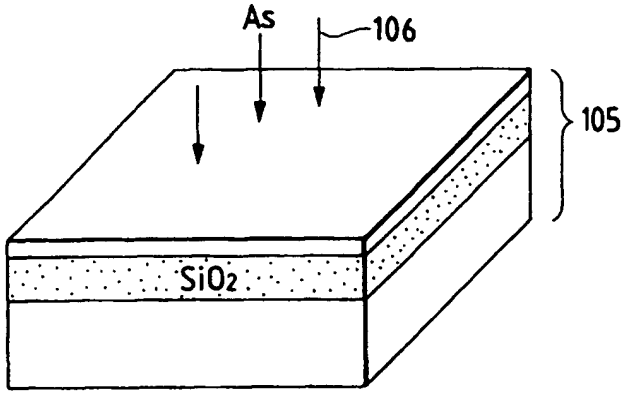


FIG. 11

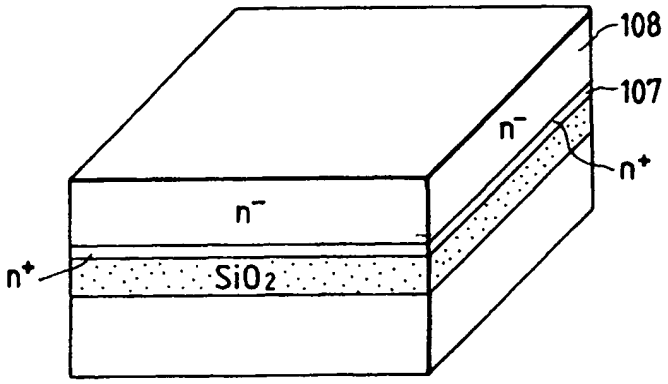


FIG. 12

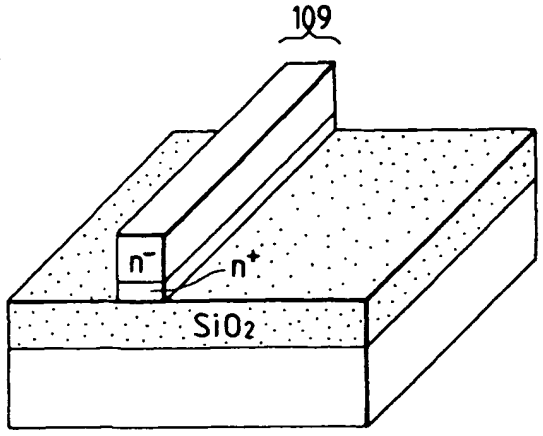


FIG. 13

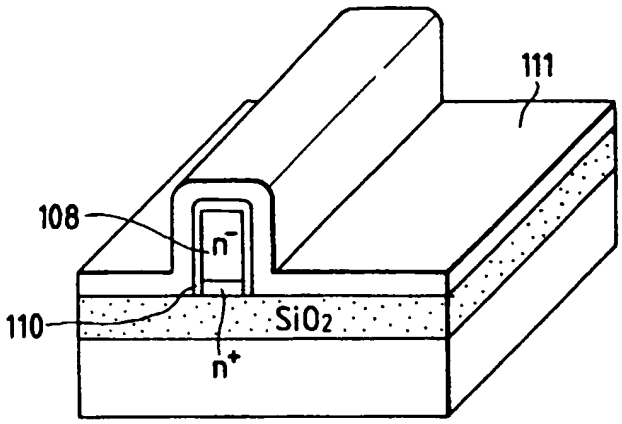


FIG. 14

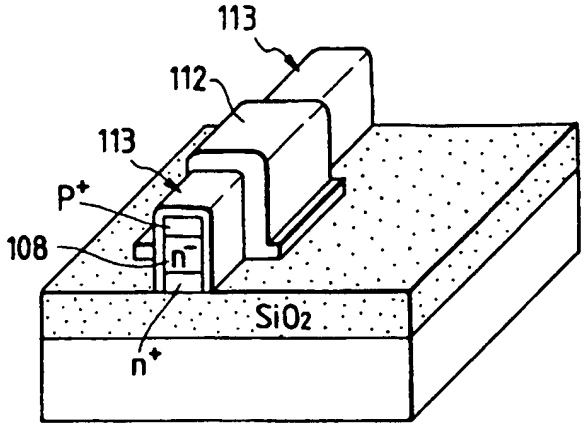


FIG. 15

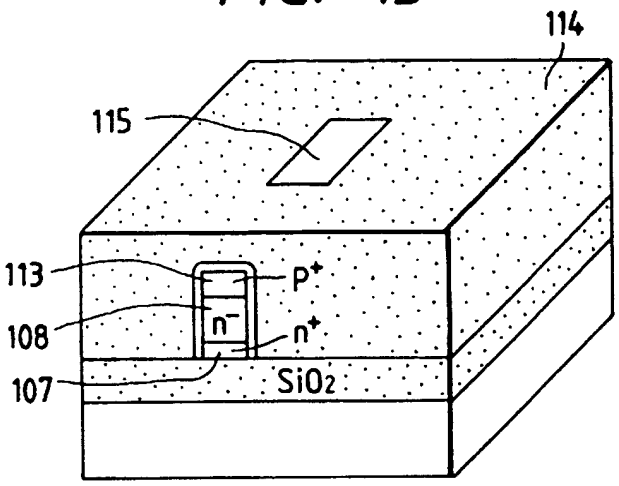


FIG. 16

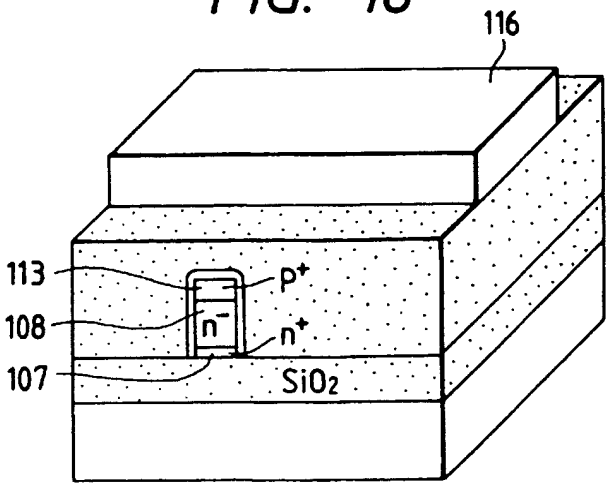


FIG. 17

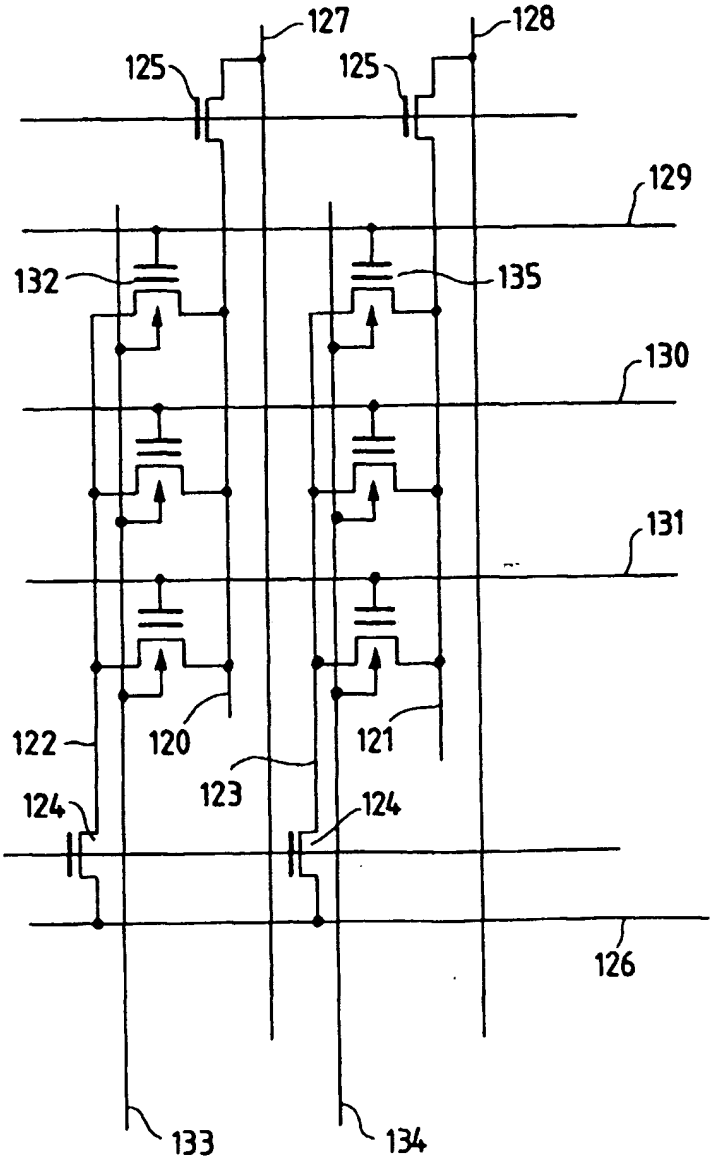

127
128
125
125
129
132
135
130
131
122
120
121
123
124
124
126
133
134

FIG. 18

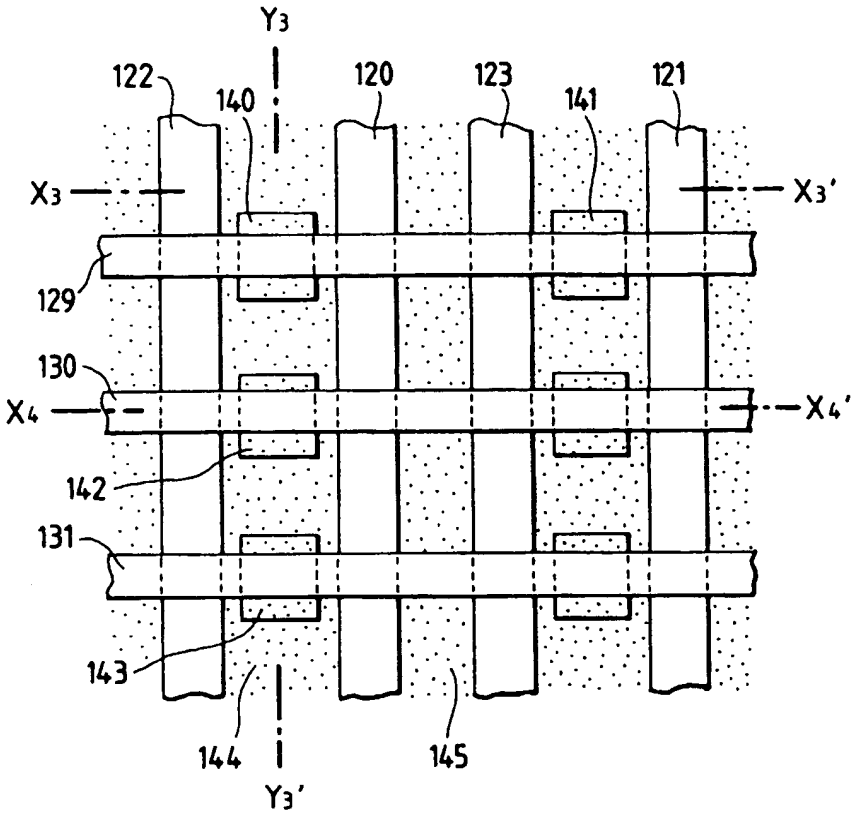

Y3
122
140
120
123
141
121
X3
X3'
129
130
X4
X4'
142
131
143
144
145
Y3'

FIG. 19

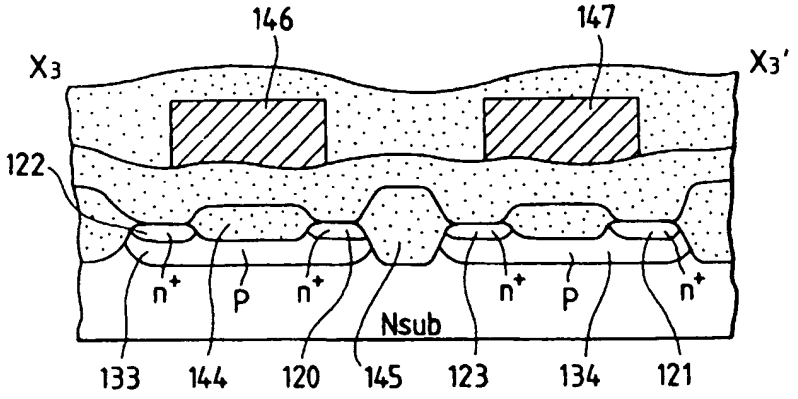

146
147
X3
X3'
122
n+
P
n+
n+
P
n+
Nsub
133
144
120
145
123
134
121

FIG. 20

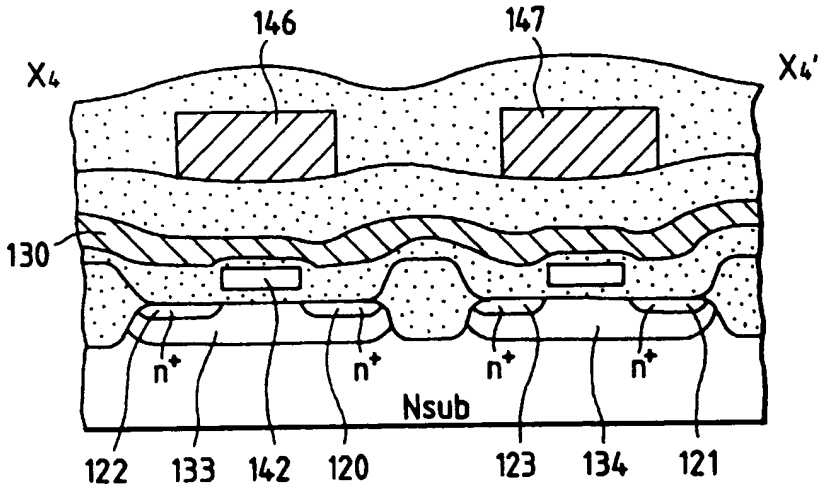

146
147
X4
X4'
130
n+
n+
n+
n+
Nsub
122
133
142
120
123
134
121

FIG. 21

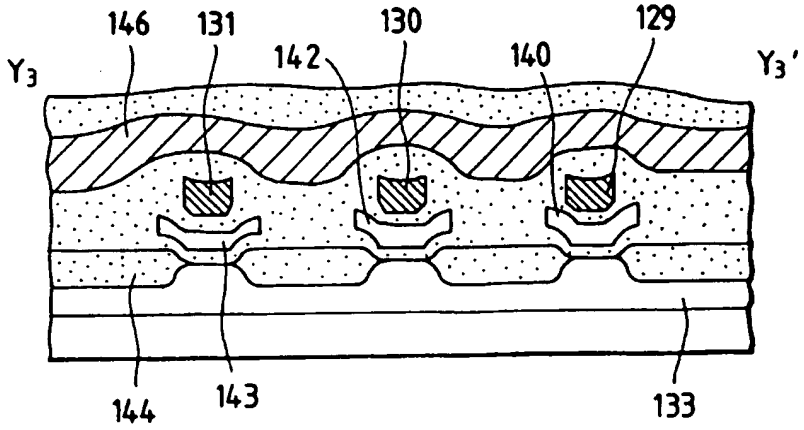
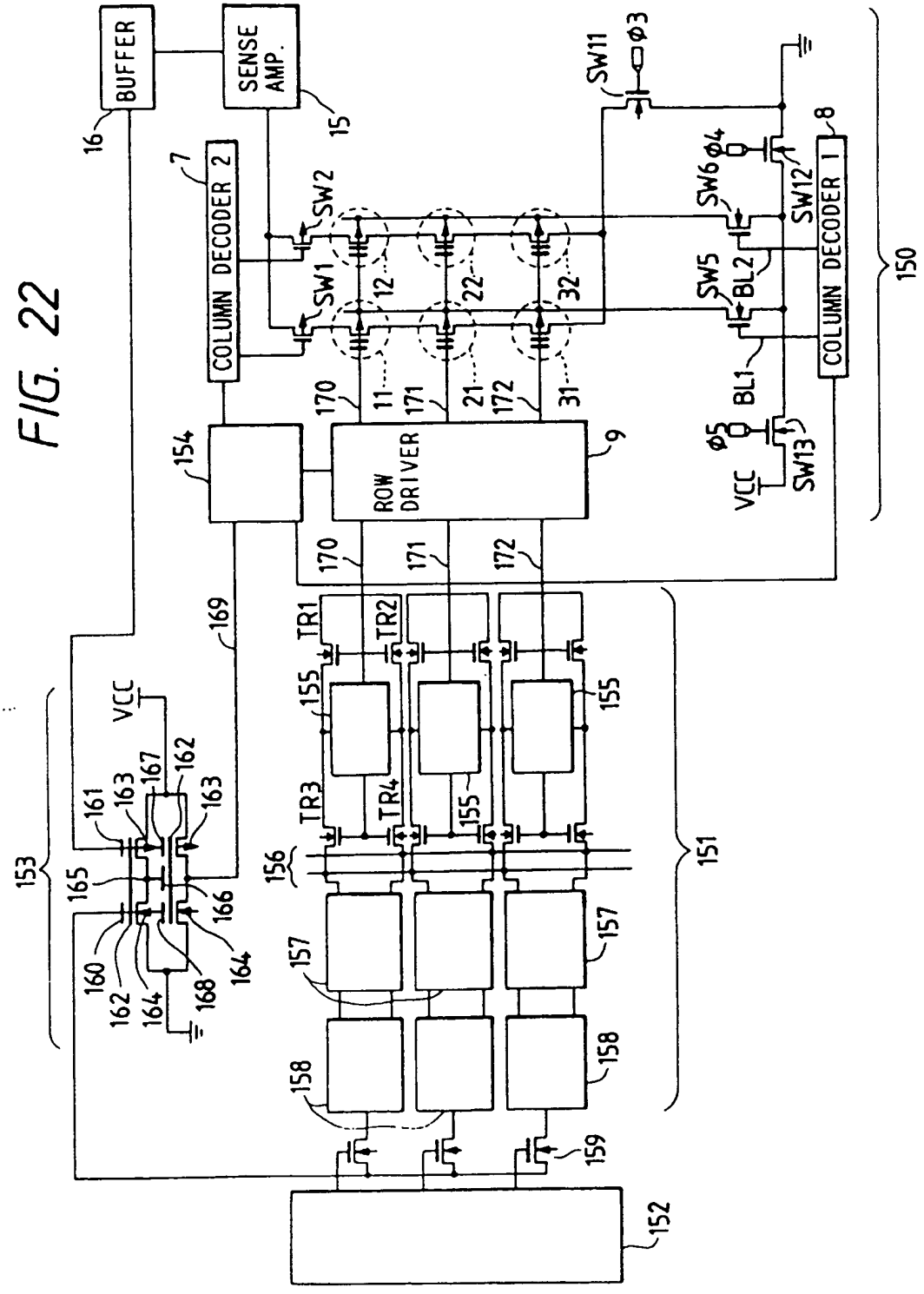

146
131
130
129
142
140
Y3
Y3'
144
143
133

FIG. 22


BUFFER
SENSE AMP.
COLUMN DECODER 2
COLUMN DECODER 1
ROW DRIVER
VCC
SW1
SW2
SW5
SW6
SW11
SW12
SW13
BL1
BL2
TR1
TR2
TR3
TR4
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
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15
16

FIG. 23

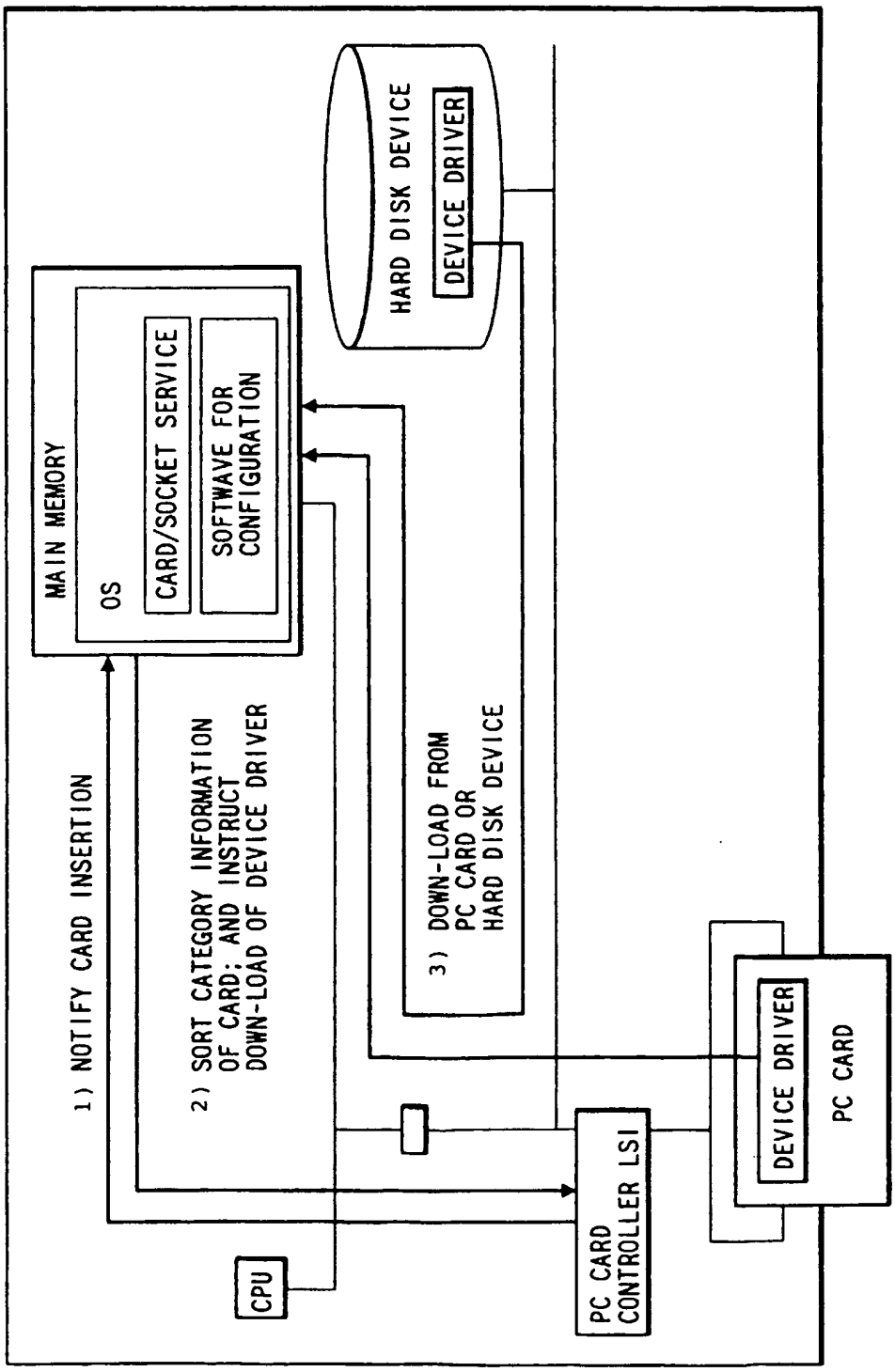
MAIN MEMORY
OS
CARD/SOCKET SERVICE
SOFTWAVE FOR CONFIGURATION
HARD DISK DEVICE
DEVICE DRIVER
1) NOTIFY CARD INSERTION
2) SORT CATEGORY INFORMATION OF CARD; AND INSTRUCT DOWN-LOAD OF DEVICE DRIVER
3) DOWN-LOAD FROM PC CARD OR HARD DISK DEVICE
CPU
PC CARD CONTROLLER LSI
DEVICE DRIVER
PC CARD

FIG. 24